NOTEBOOK SECTION

8.5-15

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2M-C183A-00

DRAWING SET NUMBER

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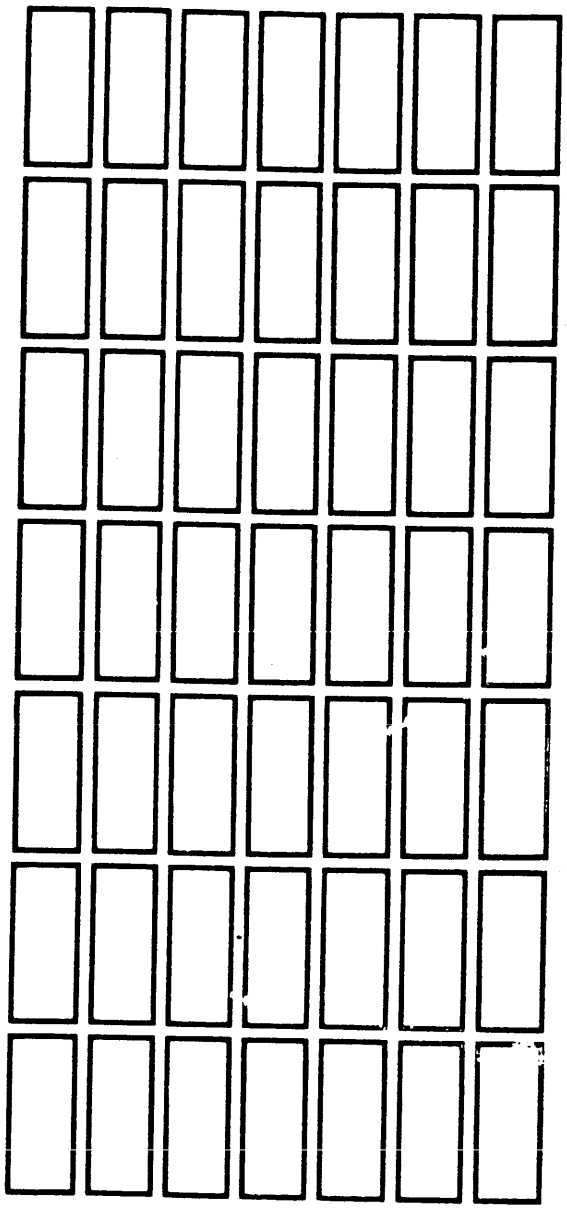
YM-C183C-00 B

DATE

DECEMBER 1981



VSV11/VS11
RASTER GRAPHICS SYSTEM

OPTION DESCRIPTION
YM-C183C-00

M207

digital

Computer Special Systems

NASHUA

1st Printing February 1981
2nd Printing (Rev) June 1981
3rd Printing (Rev) December 1

TABLE OF CONTENTS

CHAPTER 1 INTRODUCTION

CHAPTER 2 VSV11/VS11 INSTALLATION PROCEDURE

CHAPTER 3 PROGRAMMING REFERENCE

CHAPTER 4 M7064 DISPLAY PROCESSOR TECHNICAL DESCRIPTION

CHAPTER 5 M7062 IMAGE MEMORY TECHNICAL DESCRIPTION

CHAPTER 6 M7061 SYNC GENERATOR/CURSOR CONTROL DESCRIPTION

CHAPTER 7 MAINTENANCE

APPENDIX A PARTS/DATA SHEETS

APPENDIX B VRV02-BA/BB 20mA to EIA CONVERSION

APPENDIX C VT100/VRV02 SETUP and OPERATOR INFORMATION

Figures

Tables

CHAPTER 1

INTRODUCTION

1.1 GENERAL DESCRIPTION

The VSV11/VS11 is a video graphics system consisting of three quad-size modules and a joystick assembly. The system uses a high-speed microprocessor as the display processor, with a graphics instruction set that is based on the versatile VT11 instruction set. Included in the VSV11/VS11 instruction set are three bit map modes. An image memory is used in the VSV11/VS11 system to store the pixel data output of the display processor. The image memory is then continually "read" to the system monitor for the display of pixel information. The use of an image memory eliminates the need for display file refreshing and allows the display file to be changed after the first read pass. When the system is expanded with optional image memory, dynamic graphics can be run. The video output from the VSV11/VS11 system is EIA RS-170 compatible and can drive a black and white or RGB color composite video monitor. Either 50 Hz or 60 Hz, interlaced or noninterlaced scanning is provided.

There are two basic graphics systems available: the VSV11 for use with an LSI-11 CPU host, and the VS11 for use with a PDP-11 host. The difference between the two is that the VS11 system includes a DW11 UNIBUS-to-LSI-11 Bus Converter. Both systems employ three modules which plug into an "H9273-type" backplane. This type backplane has LSI-11 busing on the A-B slots and daisychain or video busing on the C-D slots. Since the VS11 system includes the DW11, a backplane (DDV11-CK) is supplied for mounting into PDP-11 mounting boxes. This backplane is compatible with the VSV11/VS11 modules. VSV11 systems are not supplied with a backplane. Operating power for the VSV11/VS11 modules is supplied by the power supplies in the host CPU.

The basic three-module VSV11/VS11 graphics system has a Display Processor module (M7064), one Image Memory module (M7062) and one Sync Generator/Cursor Control module (M7061). Optional Memory and Sync Generator modules can be used to expand the basic system for multi channel and/or multi monitor operation. One image memory module provides one memory channel with either 512 X 512 X 2 bits or 512 X 256 X 4 bits of pixel resolution and intensity. Additional image memory modules can be added to provide for:

1. Single memory channel with 512 X 512 X 4 bits of pixel resolution and intensity for one system monitor, with no dynamic graphics.

2. Two memory channels each with 512 X 256 X 4 bits of resolution and intensity for one monitor with dynamic graphics.

3. A four memory channel system, each channel having 512 X 512 X 2 bits of resolution and intensity; paired channels would drive separate monitors, each monitor could display independent dynamic graphics, and

4. Four separate channels, each channel having either 512 X 256 X 4 bits or 512 X 512 X 2 bits of resolution and intensity for four independent monitors with no dynamic graphics. Optional M7061 Sync Generator modules are required for each additional independent system monitor.

In summary, the VSV11/VS11 has the following features:

- VT11-type instructions including Vector, Point, Graphplot, Run-length, and Bitmap modes.

- LSI-11 Bus NPR capability, with 18-bit addressing.

- Modules operate in DDV11-CK & H9273 type backplane.

- Resolution of 512 X 256 X 4 bits or 512 X 512 X 2 bits, switch-selectable (with one memory).

- Outputs 4 or 16 grey levels, or 16 colors.

- Video output for VT100 (Maximum of one VT100 per VSV11/ VS11 subsystem).

- Can sync to an external RS-170 source having equal number of scan lines as Sync Generator.

- Mixes video from an external RS-170 source.

- Software- and Joystick-controlled cursor, supplied with a rate-type joystick; cursor size and intensity is jumper-selectable between two choices.

- Multi-channel and/or multi-monitor operation.

- Compatible with analog monochrome or RGB-COLOR monitors requiring EIA RS-170 composite sync.

- 50 Hz or 60 Hz, interlaced or noninterlaced operation.

- Software-controlled hardware blink.

1.2 BASIC FUNCTIONAL DESCRIPTION

Figure 1-1 is a block diagram of the VSV11/VS11 graphics system. Three major functions appear on this diagram. These are:

(1) the M7064 Display Processor (abbreviated DPU),
(2) the M7062 Image Memory, and
(3) the M7061 Sync Generator/Cursor Control.

These three major functions are the three modules of the VSV11/VS11 system. Figure 1-1 shows the optional additional M7062 Image Memory. The H3060 joystick is supplied with all systems, and the DW11 is used only with the VS11 system.

The system modules interface to each other by means of two internal buses. These buses are the DBUS (Memory Data Bus) and the VBUS (Video Bus). The DBUS is a three-state bus that carries pixel data and control signals between the M7064 Display Processor and the M7062 Image Memory, and between the Display Processor and the M7061 Sync Generator/Cursor Control. Physically, the DBUS is a 40-conductor ribbon cable with Berg-type connectors. The cable is connected from the 40-pin Berg-type connector on the Display Processor module to the 40-pin Berg-type connectors on each Memory and Sync module. The Video Bus is a three-state bus (only two-states are used) interfacing the Display Processor, Memory, and Sync modules. This bus carries sync and timing signals and video pixel data. Physically, the video bus is the daisy-chain wiring on the C-D slots of an H9273-type or the E-F slots of a DDV11-CK backplane. A complete description of the DBUS is presented in Chapter 5, while the Video Bus is detailed in Chapter 6.

The VSV11/VS11 system operates as a DMA device on either the LSI-11 or PDP-11 bus. After constructing a display file in the CPU memory, the starting address of the file is transferred to the Display Processor's Display Program Counter (DPC). The Display Processor then makes nonprocessor requests (NPRs) to gain use of the bus. Once bus master, the Display Processor has direct memory access (DMA) to the CPU memory for reading the display file. Display file instructions consist of Graphic, Control, and Data instructions (these are fully explained in Chapter 3). These instructions are processed by the Display Processor and set-up the graphic mode, status registers and control functions, and contain the pixel (picture element) information for display. Picture information processed by the Display Processor is sent to the Image Memory via the Memory Bus/DBUS for storage and eventual display on the system monitor. A detailed description of the Display Processor is presented in Chapter 4.

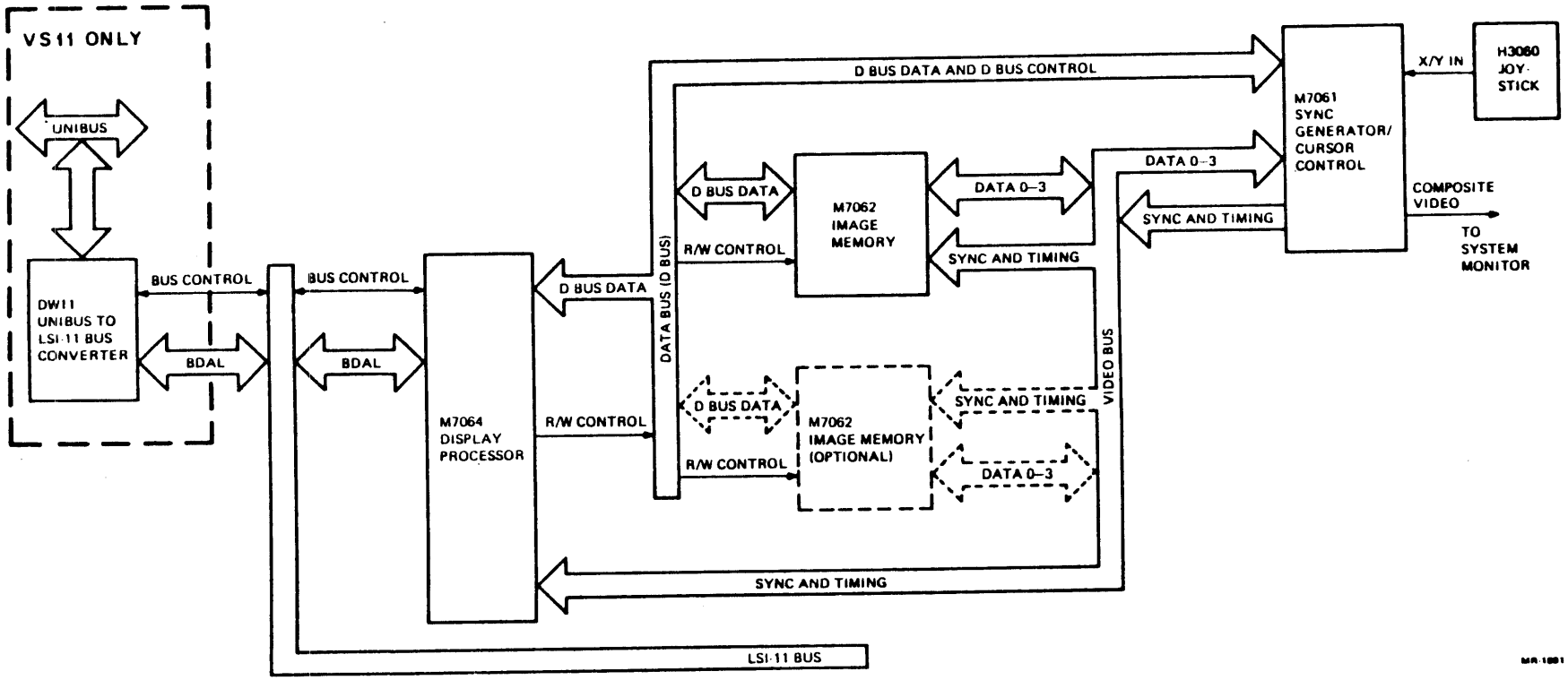


Figure 1-1
VSV11/VS11 Graphics System Block Diagram

The Image Memory stores an "image" of the pixel information to be displayed on the system monitor. Pixel data received from the Display Processor is stored in thirty-two 16K Random Access Memories (RAMs) on the M7062. X and Y address lines to the RAMs control which pixel position is to be written or read. RAM X and Y addresses correspond to pixel X and Y coordinates on the screen of the system monitor. Digital data for display is read from the M7062 to the M7061 Sync Generator/Cursor Control via the Video Bus (VBUS). At the M7061, the digital data is converted to analog data. Because the Image Memory stores the picture to be displayed, the display file in the CPU memory is not required for refreshing the display and can be changed after its contents are transferred to the VSV11/VS11. Optional M7062 Image Memory modules can be added to the basic VSV11/VS11 system to increase pixel resolution, to run dynamic grahics, or for multi-monitor and/or multi-channel operation. Chapter 5 presents a detailed description of the M7062 Image Memory.

The M7061 Sync Generator/Cursor Control provides digital-to-analog conversion of the pixel data from the M7062 Image Memory for display on the system monitor. Sync and blanking pulses generated by the M7061 are used throughout the VSV11/VS11 system and are combined with the pixel video data to produce the EIA RS-170 composite video signal for the monitor. Cursor control circuits within the M7061 compute positions for display on the system monitor based on one of three data inputs. The joystick, PDP11 I/O, or display file primitive can all control the displayed cursor position. Match and Switch interrupts (explained in Chapter 3), originated by pressing the joystick interrupt switch or actuated by software, are controlled by logic on the M7061. Joystick position is read back to the Display Processor via the Memory Bus/DBUS during a switch interrupt. The joystick itself consists of an X-position and a Y-position potentiometer, and two interrupt switches wired in parallel. These components are mounted in an enclosure which connects to the M7061 module via a cable. The H3060 joystick is referred to as a rate-type joystick. That is, small movements of the joystick produce slow movements of the crosshairs. Large joystick movements cause the crosshairs to move rapidly. Detailed descriptions of the M7061 Sync Generator/Cursor Control module and the H3060 Joystick are provided in Chapter 6.

The DW11 UNIBUS-to-LSI-11 Bus Converter is supplied only with VS11 systems. The converter translates UNIBUS and LSI-11 Bus signals. This translation is required because the Display Processor is an LSI-11 Bus device, and VS11 systems are used with PDP-11 host CPUs. Complete details on the DW11 are presented in the DW11 UNIBUS to LSI-11 Bus Converter Installation Guide (EK-DW11A-IN).

1.3 OPTION DESIGNATIONS

Various standard VSV11 and VS11 option packages are available. The standard "packaged" units are based upon the VSV11-AA, which is a 3-module set containing one M7064 Display Processor, one M7061 Sync Generator/Cursor Control, and one M7062 Image Memory (also called a Frame Buffer). VSV11 systems, for LSI-11 Bus systems, plug directly into an LSI-11 Bus backplane (H9273-A or equivalent); the backplane is not supplied. VS11 systems, for PDP-11 and VAX UNIBUS systems, include a DW11-BK UNIBUS-to-LSI-11 Bus Converter, which includes a 4-slot backplane. The basic VSV11 or VS11 logic can be augmented with one addition M7062 Image Memory as part of the standard offering.

Some packages do not include a display monitor. Others include either a 12" Monochrome (Black & White) monitor (VT100-LA/LB) or a 19" Color monitor (VRV02). Both types of monitors are based upon the VT100 terminal. The VT100-LA (120V/60Hz) or VT100-LB (240V/50Hz) is a standard VT100-AA with a P40 phosphor and anti-glare shield. The VRV02-BA (120V/60Hz) or VRV02-BB (240V/50Hz) are composed of two free-standing units plus a detachable keyboard. One of the units is a 19-inch (diagonal measure) color CRT. The other is a Keyboard Interface containing standard VT100 logic and a power supply. Both types of standard monitors can communicate with the host CPU over a standard serial line and can function as a standard terminal. The serial line does not connect to the VSV11/VS11 logic; the user must provide a standard interface for communications (DZ11, DL11, etc.)

In addition to the standard units, VSV11/VS11 "building blocks" are available for constructing "extended" graphic systems. These extended systems can contain multiple Memory and Joystick channels, providing for high-resolution "dynamic" displays and/or attachment of multiple independent display monitors.

Table 1-1 lists the standard VSV11 and VS11 graphic systems designations. Table 1-2 lists the model designations of the VSV11/VS11 building blocks.

Table 1-1
VSV11 and VS11 Graphics System Designations

DESIGNATION				No. of Image Memories	Display Monitor
LSI-11 Bus		UNIBUS			
120V/60Hz	240V/50Hz	120V/60Hz	240V/50Hz		
VSV11-AA	VSV11-AB	VS11-AA	VS11-AB	1	None
VSV11-AC	VSV11-AD	VS11-AC	VS11-AD	2	None
VSV11-AE	VSV11-AF	VS11-AE	VS11-AF	1	VT100 (B&W)
VSV11-AH	VSV11-AJ	VS11-AH	VS11-AJ	2	VT100 (B&W)
VSV11-AP	VSV11-AR	VS11-AP	VS11-AR	1	VRV02 (Color)
VSV11-AS	VSV11-AT	VS11-AS	VS11-AT	2	VRV02 (Color)

Table 1-2
VSV11/VS11 Building Block Model Designations

DESIGNATION		DESCRIPTION
60 Hz	50 Hz	
VSV11-BA	VSV11-BB	VSV11-AA/AB plus DDV11-DK 9-Slot Backplane, Power Harness Adapter, Six G7272 Grant Continuity Cards, Extended DBUS Data Cable, and M9403 LSI-11 Bus Connector with +15V to +12V Converter.
VS11-BA	VS11-BB	VSV11-AA/AB with DW11-EK UNIBUS to LSI-11 Bus Converter. Equivalent to VS11-AA/AB but with DDV11-DK 9-Slot Backplane.
VS11-BC	VS11-BD	VSV11-AA/AB with DW11-A UNIBUS to LSI-11 Bus Converter. The DW11-A contains an M8217 bus converter module, an M9401 bus connector, and two BC05L-16 16-foot 40-conductor ribbon cables. With the addition of an H9273-A backplane and LSI-11 expansion box, such as BA11-N, this building block can be used on a UNIBUS system.
VSV11-MA		M7062 Image Memory Module
VSV11-SA	VSV11-SB	M7061 Sync Generator/Cursor Control Module plus Video Cables
VSV11-SC	VSV11-SD	M7061 Sync Generator/Cursor Control Module, Video Cables, and Joystick Pigtail Cable
VSV11-SE	VSV11-SF	M7061 Sync Generator/Cursor Control Module, Video Cables, and Multi-Tap Joystick Pigtail Cable (for connecting a single H3060 Joystick to up to four M7061 modules)
H3060		Joystick Assembly
VT100-LA	VT100-LB	Monochrome Monitor Terminal (same as VT100-AA/AB but with P40 phosphor)
VRV02-AA	VRV02-AB	19-inch Color Monitor (with no Keyboard or terminal logic)
VRV02-BA	VRV02-BB	19-inch Color Monitor Terminal (with Keyboard and terminal logic)

1.4 SPECIFICATIONS*

1.4.1 Environmental Requirements

Temperature	
Storage	-40°to 66°C (-40°to 150°F)
Operating	5°to 50°C (40°to 120°F)
Relative Humidity	10% to 95% noncondensing

1.4.2 Logic Power Requirements

		Nominal	Max.
M7064	+5V	2.8 Amp	3.0 Amp
M7062	+5V	1.2 Amp	1.5 Amp
	-5V**	0.006 Amp	0.01 Amp
	+12V	0.45 Amp	0.5 Amp
M7061	+5V	1.2 Amp	1.5 Amp
	+12V	0.11 Amp	0.15 Amp
VSV11	+5V	5.2 Amp	6.0 Amp
	+12V	0.56 Amp	0.65 Amp
M8217	+5V	2.5 Amp	3.0 Amp
M9403	+15V	Equal to +12Vdc current drawn by M7061 and M7062 modules.	

** Supplied by M7061

1.4.3 Sync Generator (M7061)

(M7061 operating from crystal oscillator)

Horizontal Frequency	15.734 kHz ± 0.2%	
Scan Lines Per Frame		
60HZ Interlaced	525	
60HZ Noninterlaced	525	
50HZ Interlaced	629	
50HZ Noninterlaced	629	
Visible Lines Per Field		
60HZ Interlaced	480	(2x240/Field)
60HZ Noninterlaced	240	(1x240/Field)
50HZ Interlaced	512	(2x256/Field)
50HZ Noninterlaced	256	(1x256/Field)

* Specifications are subject to change without notice.

1.4.3.1 Video Output To VT100 -

Output Video Voltage	1.2Vp-p, ± 20%
Output Impedance	75 ± 5%
Video (Rise, Fall)	25ns max
Sync (Rise, Fall Time)	25ns max

[Video signal derived from Monochrome/Green (Composite Video) output, but without mixed video input.]

1.4.3.2 Monochrome/Green, Red, Blue Video Outputs -

(Red and Blue unconnected and unterminated will cause both the VT-100 and the Monochrome/Green (Composite Video) outputs to provide 16 levels of video.)

Monochrome operation with 16 grey shades
(Red and Blue unterminated)

Monochrome(/Green) output (From Composite Video Output)	EIA RS-170 compatible Composite Sync with 16 video levels and mixed video input.
Sync (Figure 1-2)	EIA RS-170 Compatible
Sync Voltage	0.4V ± 20%
Video Voltage, max (Figure 1-3)	1.2VP-P ± 20%
Output Impedance	75 ohms ± 10%
Signal Transition Times (Figures 1-2 and 1-3)	
Sync (Rise, Fall Time)	25ns max
Video (Rise, Fall Time)	25ns max
Red output	Unconnected and Unterminated
Blue output	Unconnected and Unterminated

RGB operation with 16 colors
(Red and Blue terminated by 75 ohms)

(Monochrome/)Green Output (from Composite Video Output)	EIA RS-170 compatible Composite Sync with 4 video levels, and mixed video input.
Sync (Figure 1-2)	EIA RS-170 Compatible
Sync Voltage	0.4V ± 20%
Video Voltage, Max. (Figure 1-3)	1.2VP-P ± 20%
Output Impedance	75 Ohms ± 10%
Signal Transition Times (Figures 1-2 and 1-3)	
Sync (Rise, Fall Time)	25ns max
Video (Rise, Fall Time)	25ns max
Red Output:	Low = 0.21 V max
2 video levels	High = 0.93 V ± 20%
Output Impedance	
High State	330 Ohms ± 10%
Low State	30 Ohms max
Signal Transition Times (Figures 1-2 and 1-3)	
Video Risetime	50ns max
Video Falltime	25ns max
Blue Output:	Low = 0.21 V max
2 video levels	High = 0.93 V ± 20%
Output Impedance	
High State	330 Ohms ± 10%
Low State	30 Ohms max
Signal Transition Times (Figures 1-2 and 1-3)	
Video Risetime	50ns max
Video Falltime	25ns max

1.4.3.3 Video Input & Mixer Requirements -

Video Input Waveform	RS-170
Input Frequency Range	15.734 kHz ± 1%
Input Voltage Range	
Sync (Negative)	0.4V ± 30%
Video (Positive)	1.0V ± 30%
Input Impedance	75 ± 5%
Bandwidth (Video Input To Video Output)	10 MHz
Mixer Function	Video Input is OR'ed with internally generated signal. Result is fed out through Composite (Monochrome/Green) Output and does not appear on the VT100 output.
Video Input Registration	See Figure 1-4

1.4.4 Image Memory (M7062)

Image Memory Resolution	512x512x2 Bits or 512x256x4 Bits
Output Pixel Rate	1 Pixel per 80 nsec.
Bits Per Pixel	2 or 4
Input Data Rate to Image Memory	1 Pixel per 640 nsec max
Pixel Timing, Per Line	See Figure 1-4
Visible Lines Timing	See Figure 1-5

1.4.5 Display Processor I/O (M7064)

Data Transfer Mode	LSI-11 Bus NPR's
Bus Loading	1 Bus Load
Instruction Set	See Chapter 3

1.4.6 Monitor Specifications

1.4.6.1 VT100-LA/LB -

Type	Monochrome (Black & White)
Size	12-inch, diagonal screen measure
Phosphor	P40
Power	
VT100-LA	90-128 Vac @ 2.2 Amp
VT100-LB	180-256 Vac @ 1.1 Amp

1.4.6.2 VRV02-AA/AB -

Type	Color, R-G-B
Size	19-inch, diagonal screen measure
Phosphor	Long-Persistence
Power	
VRV02-AA	108-132 Vac @ 1.1 Amp
VRV02-AB	216-264 Vac @ 0.6 Amp

1.4.6.3 VRV02-BA/BB -

Type	Color, R-G-B w/ Keyboard & Interface
Size	19-inch, diagonal screen measure
Phosphor	Long-Persistence
Power	
VRV02-AA	
CRT	108-132 Vac @ 1.1 Amp
Keyboard Intf.	90-128 Vac @ 1.5 Amp
VRV02-AB	
CRT	216-264 Vac @ 0.6 Amp
Keyboard Intf.	180-256 Vac @ 0.8 Amp

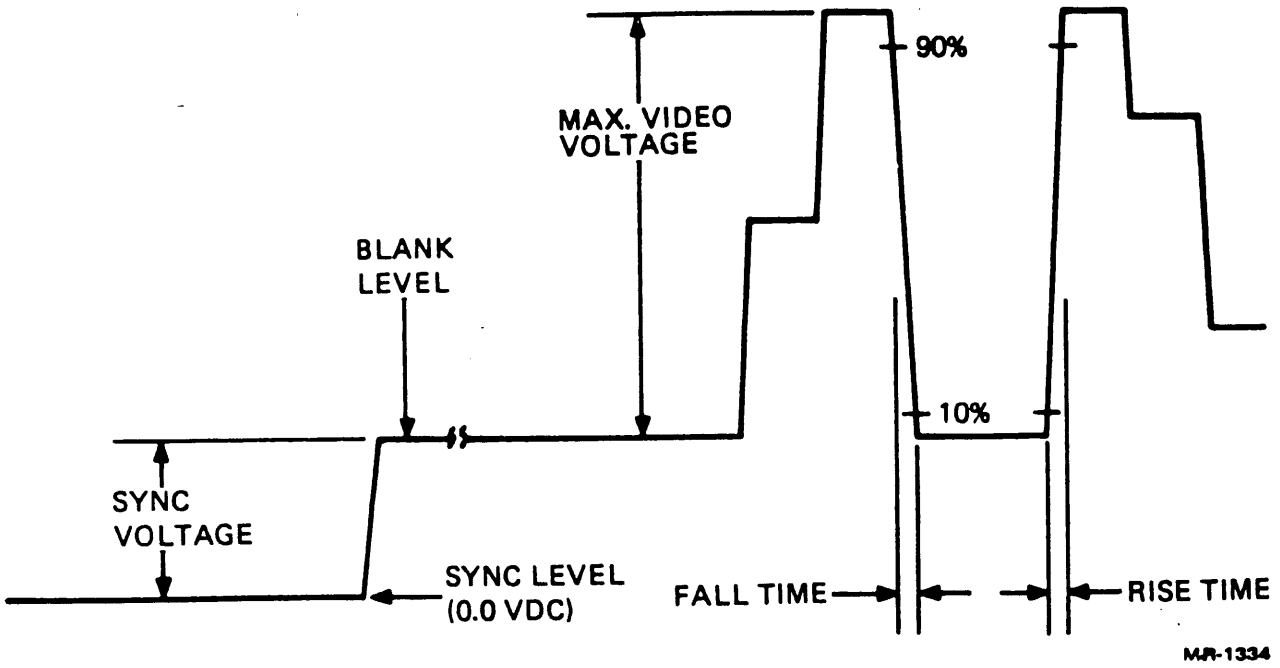


Figure 1-2
Composite Video Output Waveform

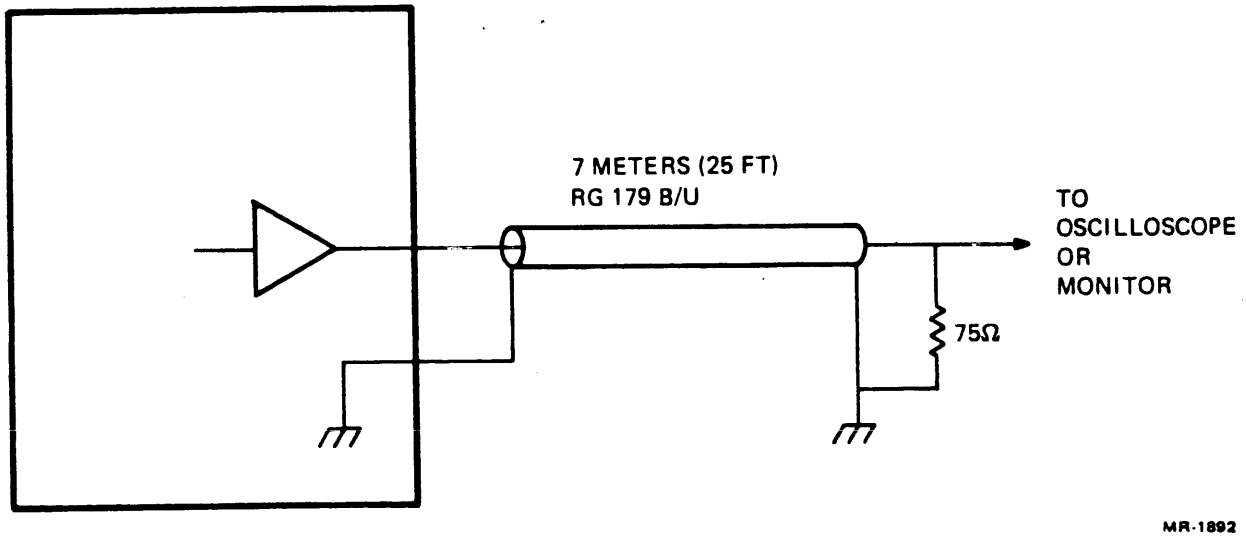
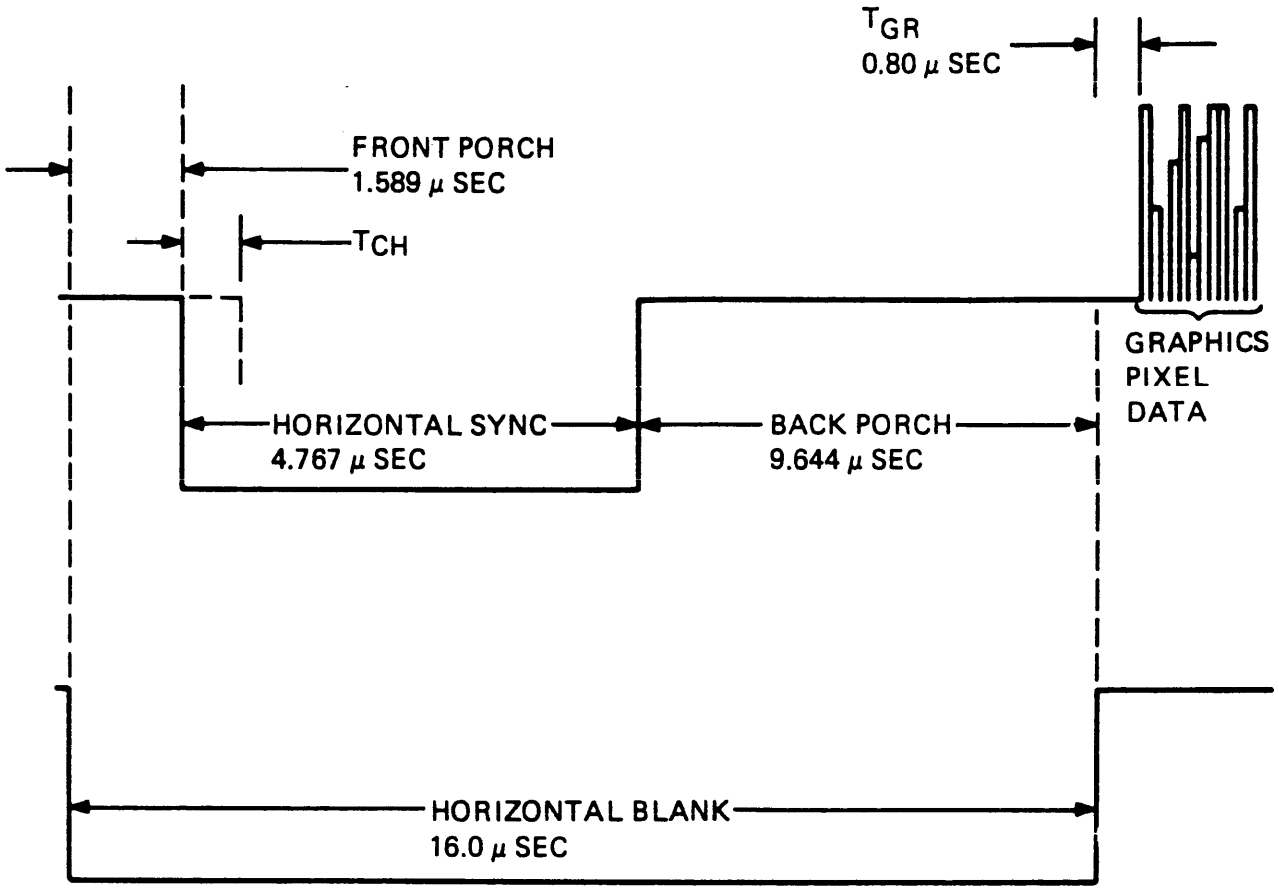


Figure 1-3
Composite Video Test Setup



T_{CH} = DELAY TIME BETWEEN LEADING EDGE OF GRAPHIC SYNC AND EXTERNAL SYNC APPLIED AT VIDEO MIXER INPUT.

T_{GR}= DELAY TIME BETWEEN LEADING EDGE OF H. BLANK TO LEADING EDGE OF FIRST GRAPHICS PIXEL.

MR-1336

Figure 1-4
External Video Input Registration

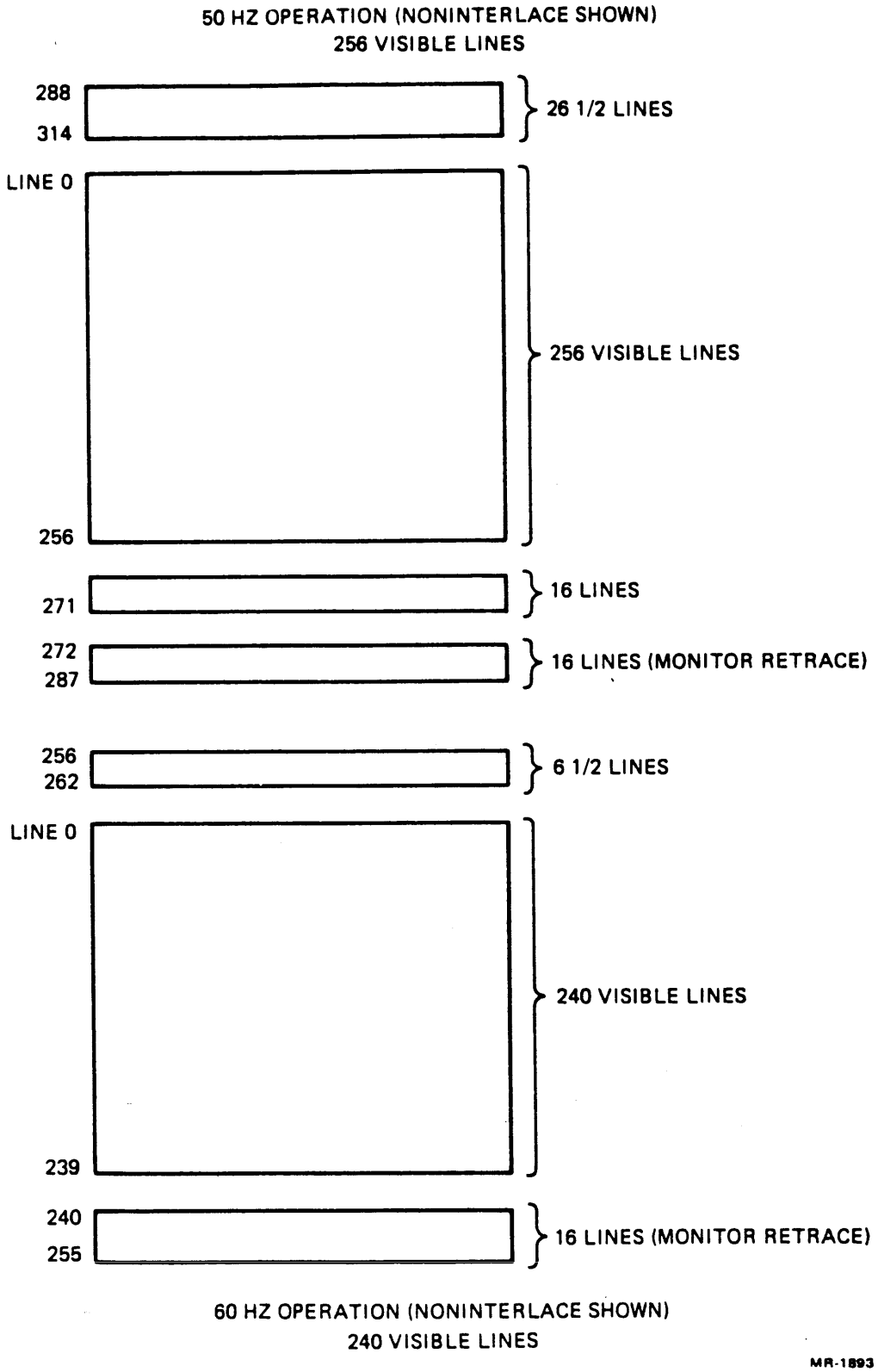


Figure 1-5
System Monitor Visible Lines - 50/60 Hz
(Noninterlaced Operation)

1.5 RELATED DOCUMENTS

The publications listed in Table 1-3 supplement the information in this manual.

Table 1-3
Related Publications

Publication	Document Number	Remarks
VSV11 Field Maintenance Print Set	B-TC-VSV11-0-1	Shipped with Unit
VS11 Field Maintenance Print Set	B-TC-VS11-0-1	Shipped with Unit
VT100 User Guide	EK-VT100-UG	Available in Hard Copy **
VT100 Technical Manual	EK-VT100-TM	In Microfiche Library;* Available in Hard Copy **
DW11 UNIBUS-to-LSI-11 Bus Converter Installation Guide	EK-DW11A-IN	In Microfiche Library;* Available in Hard Copy **
Installation, Operation and Maintenance Manual for Model HM-2719/2713 Color Monitor	-	Hitachi Publication. Shipped with Color Systems

* For information concerning microfiche libraries contact:

Digital Equipment Corporation
132 Parker Street
Maynard, MA 01754

**These documents can be ordered from:

Digital Equipment Corporation
444 Whitney Street
Northboro, MA 01532

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CHAPTER 2

VSV11/VS11 INSTALLATION PROCEDURE

The procedures in this Chapter are provided to allow the Field Engineer to successfully install a VSV11 Graphic System on an LSI-11 computer system or a VS11 Graphic System on a PDP-11 or VAX-11 system.

The detailed step-by-step procedure given in the following paragraphs applies to all standard VSV11/VS11 models which contain only one M7061 Sync Generator module and one or two M7062 Image Memory modules. For special "extended" configurations, containing 2 or more Sync Generator modules or 3 or more Image Memory modules refer first to Paragraph 2.8. Installation of these extended configurations can be carried out one memory/sync channel at a time, using the detailed procedures given in Paragraphs 2.1 through 2.6.

The procedures given below standardize the installation and setup of VSV11/VS11 systems such that any basic system, whether it uses one or two memory modules or must be set up to special customer requirements, will contain one memory channel capable of displaying 16 colors or intensities. For the case of a single Image Memory module, illustrated in the block diagram of Figure 2-1, the mode will be Non-Interlaced, with the memory supplying 4 bits of pixel data in a 512 x 256 array. With two image memory modules, shown in Figure 2-2, the mode will be Interlaced, with each memory module supplying 2 bits of the 4 bits of pixel data in a 512 x 512 pixel array. Furthermore, standard settings for blink rate, cursor size and color, and operating frequency are used during initial installation. After the system is successfully installed using the standard setups, various optional changes can be made to tailor the system to customer needs (Paragraph 2.6). The use of a standard initial setup will facilitate troubleshooting should trouble occur.

In order to install the standard units, the following steps are performed; they are covered in detail in the succeeding paragraphs:

1. Unpack and inventory the components.

2. Inspect the computer system and verify that appropriate space and power are available; also determine device and vector addresses to be used.

3. Prepare the display monitor (if supplied) by verifying ac power selection. Then, use the keyboard SET-UP functions to set initial operating parameters.

4. Verify and/or set up the switches and jumpers on the logic modules to standard settings. (During initial installation, the system is set up to have one memory channel supplying 16 levels of color or intensity; standard settings are also used for Cursor size and color, and for Blink rate. After initial checkout, customer changes can be made.)

5. If the unit is a VS11, install the DDV11-CK backplane and UNIBUS-to-LSI-11 Bus Converter.

6. Perform initial shorts and power checks.

7. Install the logic modules and DBUS Data Cable.

8. Connect the Display Monitor and Joystick to the logic modules.

9. Check out the system using the supplied diagnostic programs.

10. If necessary, perform customer-requested set-up of optional functions via reconfiguration of switches and jumpers on the logic modules; check these out using the diagnostic program.

11. Perform final routing of cables and secure mounting box covers.

12. Perform unit acceptance using the diagnostic program.

Perform the installation by executing in sequence each of the activities described in the following paragraphs. If trouble is encountered during any step, refer to the troubleshooting procedures in Chapter 7.

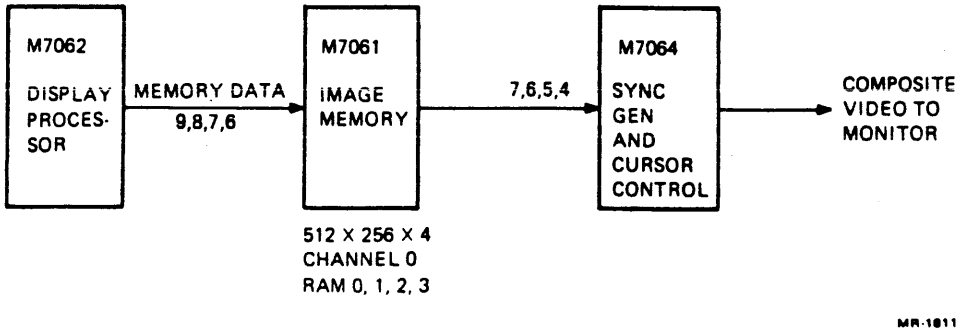


Figure 2-1
Single-Memory Non-Interlaced Installation Block Diagram

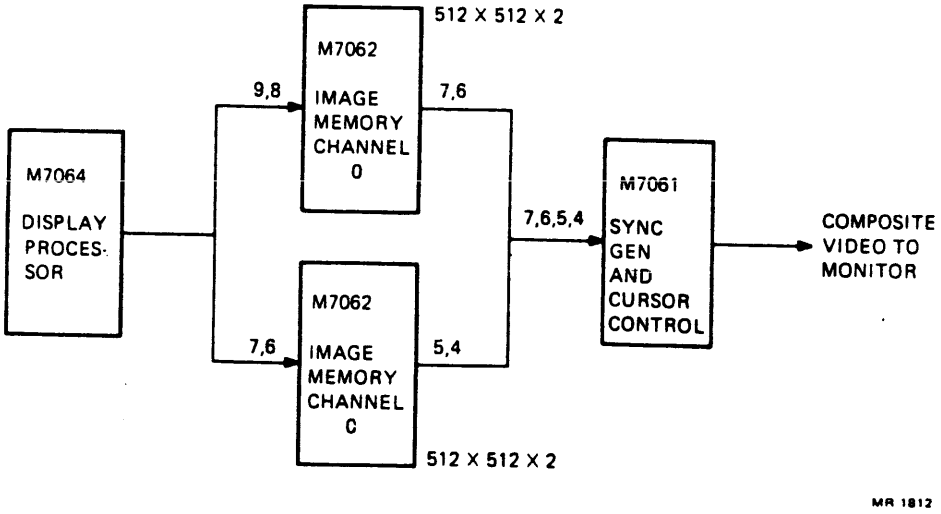


Figure 2-2
Two-Memory Interlaced Installation Block Diagram

2.1 UNPACKING & INVENTORY

A. Obtain the Shipping List for the VSV11 or VS11 model at hand and verify that it is what the customer ordered.

B. Open each carton.

C. Turn to Appendix A of this manual and find the Parts/Data sheet for the VSV11 or VS11 at hand; there is one sheet for each available VSV11 or VS11 model type.

D. Unpack each carton and verify that all pieces have been received by comparing against the parts list in the appropriate Parts/Data sheet.

2.2 SYSTEM INSPECTION

A. Installation Site Considerations

The following items must be considered before the VSV11 or VS11 option can be installed:

1. Physical and Electrical placement on the bus (LSI-11 Bus or UNIBUS), with respect to:

   (a) System Compatibility (LSI-11 Bus) -- the VSV11 cannot be installed on an LSI-11 system that has options which require the use of External Memory Refresh.

   (b) NPR Priority -- place VSV11/VS11 toward end of bus if possible.

   (c) Option mounting space requirements -- refer to the appropriate Parts/Data sheet in Appendix A for physical space requirements. For example, a VSV11 option requires 3 or 4 adjacent slots in an LSI-11 Bus backplane, while a VS11 option requires a quad-height SPC slot on the UNIBUS plus space for a 4-slot, hex-height DDV11-CK backplane in the same mounting box as the aforementioned SPC slot.

2. Device Address and Interrupt Vector Address -- The VSV11 or VS11 requires assignment of four consecutive device addresses (words) in the LSI-11 Bus or UNIBUS I/O Page. It requires a block of 4 interrupt vectors (8 words total) beginning on an address evenly divisible by 16 (20 octal, having bits 3-0 = 0).

   The "standard" VSV11/VS11 device address, assigned by Digital Equipment Corporation, is 772000 for the first unit, 772010 for the second unit, etc. The VSV11/VS11

interrupt vectors are officially assigned to the "floating" address space with a rank of 17.

If, on computer systems running software designed to "Auto-configure" the interrupt vector addresses (such as VAX-VMS), a device is placed at its standard device address, the interrupt vector addresses of all other devices with lower rank in the floating vector space must be moved to higher addresses. For example, if the VS11 is added to a VAX system at its standard address (772000), the vectors on any DZ11's on the system must be moved. Therefore, in order to simplify installation it is recommended that the VS11 device registers be placed at a non-standard address and use a non-standard interrupt vector address. The following are recommended (if they are not already being used):

DEVICE ADDRESS (DPC) = 767010 (octal)
1st INTERRUPT VECTOR = 720 (octal)

3. Power Requirements

   (a) DC Power -- Refer to the appropriate Parts/Data Sheet in Appendix A.

   (b) AC Power -- The display monitor (CRT screen and associated equipment) requires a source of primary ac power with GROUND and NEUTRAL the same as the mainframe computer system. Refer to the appropriate Parts/Data Sheet in Appendix A for outlet supply requirements.

4. Monitor Placement -- The placement of the display monitor and joystick with respect to the VSV11/VS11 logic in the host computer is limited by the length of Monitor (Video) and Joystick cables supplied. Refer to the Field Maintenance Print Set to determine the length of cable supplied (typically 25 feet). Of this length, allow about 7 feet for routing of the cable within the cabinet. For example, with a 25 foot cable, the monitor can be placed up to 18 feet from the host mainframe.

5. Serial Communications Connection (if Display Monitor, VT100-LA/LB or VRV02-BA/BB is supplied as part of the VSV11 or VS11 option) -- Determine if the serial connection to the computer system will be by 20mA Current Loop (standard setup for VRV02-BA/BB) or by EIA RS-232 (standard for VT100-LA/LB). Also determine what baud rate will be used for serial communication. Verify that the appropriate customer-supplied communication cable is available.

B. Identify the mounting box destined to receive the VSV11 or VS11 logic modules (and backplane if VS11) and verify that it meets the requirements of the Considerations given above.

2.3 EQUIPMENT PREPARATION

A. Display Monitor Preparation

If no monitor is included with the VS11/VSV11, proceed directly to Paragraph B.

If the VSV11 or VS11 option being installed includes a Display Monitor (VT100-LA/LB or VRV02-BA/BB), one of the following procedures should be followed. Proceed to Step A.1 if the monitor is VT100-LA or VT100-LB; or if the monitor is VRV02-BA or VRV02-BB, proceed to Step A.2.

A.1 If VT100-LA or VT100-LB:

1. Move the unit (CRT Monochrome Display Monitor, power cord, and Keyboard) to its assigned location.

2. Check the Voltage Select switch on the rear of the unit for proper setting:

   VT100-LA: 120V
   VT100-LB: 240V

3. The standard interface is EIA RS-232 serial communications to the terminal interface on the host computer. If 20mA signal levels are required, the VT1XX-AA 20mA Current Loop Option must be ordered; refer to the VT100 USER GUIDE (EK-VT100-UG) for installation and checkout procedures.

4. Plug the coiled Keyboard connection cable into the KEYBOARD receptacle (phone jack) at the rear of the CRT Monitor cabinet.

5. Attach the power cord to the 3-pin receptacle at the rear of the CRT Monitor cabinet, and plug the other end into the designated source of primary ac power.

6. Turn the power ON with the toggle switch at the rear of the CRT Monitor cabinet and allow several seconds for warm-up.

7. Press the SETUP key on the keyboard; the recognizable SETUP frame should appear. Place the unit in LOCAL mode ("4" key) and press SETUP again. Type a few keys and verify that the corresponding characters appear on the screen.

8. Referring to the SETUP guidelines presented in Appendix C, set the monitor features according to VSV11/VS11 and user requirements. Specifically, note that the Transmit and Receive baud rates must match those that will be used for the serial communication link to the mainframe computer. Two Setup options must be specifically configured for the model of VSV11 or VS11 at hand; these are the "50/60Hz" option (last digit of the 4th option group of SETUP-B) and the "Interlace/Non-Interlace" option (last digit of the 3rd option group of SETUP-B). These must be set up as shown in Table 2-1.

Table 2-1
VT100-LA/LB Set-Up

Model	50/60Hz	Interlace/Non-Interlace
VSV11-AE VS11-AE	60Hz (4 xxxO)	Non-Interlace (3 xxxO)
VSV11-AF VS11-AF	50Hz (4 xxx1)	Non-Interlace (3 xxxO)
VSV11-AH VS11-AH	60Hz (4 xxxO)	Interlace (3 xxx1)
VSV11-AJ VS11-AJ	50Hz (4 xxx1)	Interlace (3 xxx1)

9. When all SETUP parameters have been selected, press the "SHIFT" and "S" keys simultaneously (while still in SETUP mode) to store the parameters.

10. Proceed to Paragraph B.

A.2 If VRV02-BA or VRV02-BB:

1. Move the unit (CRT Color Display Monitor, Keyboard Interface Assembly, two power cords, and Keyboard) to its assigned location.

2. The standard interface is 20mA serial communications to the terminal interface on the host computer. If EIA RS-232 signal levels are required, turn to Appendix B and follow the conversion procedure described there.

3. Check the Voltage Select switch on the rear of the Keyboard Interface unit for proper setting:

   VRV01-BA: 120V
   VRV02-BB: 240V

4. Plug the coiled Keyboard connection cable into the receptacle (phone jack) at the lower right on the front of the CRT Monitor cabinet.

5. Connect the cable exiting the rear of the CRT Monitor cabinet to the KEYBOARD jack on the Keyboard Interface unit.

6. The CRT Monitor and the Keyboard Interface are each supplied with an ac power cord. Connect the respective power cord to the rear of each unit (3-pin receptacle) and to the source of ac power. Note again that the Ground and Neutral conductors of the ac outlets must be the same as those for the mainframe computer system.

7. Obtain the 4-conductor Monitor Coaxial cable assembly (with BNC connectors on both ends) and identify the conductor marked with the black band. Temporarily connect this conductor between the VIDEO OUT BNC jack on the Keyboard Interface unit and one of the GREEN inputs on the rear of the CRT Monitor cabinet.

8. Make sure that the two toggle switches on the rear of the CRT Monitor cabinet are both UP ("75 OHM" and "COMP. SYNC").

9. Turn the power ON with the toggle switch at the front of the CRT Monitor cabinet and the toggle switch on the Keyboard Interface unit. Allow several seconds for warm-up.

10. Press the SETUP key on the keyboard; the recognizable SETUP frame should appear. Place the unit in LOCAL mode ("4" key) and press SETUP again. Type a few keys and verify that the corresponding characters appear on the screen.

11. Referring to the SETUP guidelines presented in Appendix C, set the monitor features according to VSV11/VS11 and user requirements. Specifically, note that the Transmit and Receive baud rates must match those that will be used for the serial communication link to the mainframe computer. Two Setup options must be specifically configured for the model of VSV11 or VS11 at hand; these are the "50/60Hz" option (the last digit of option group 4 under SETUP-B) and the "Interlace/Non-Interlace" option (the last digit of option group 3 under SETUP-B). These must be set up as shown in Table 2-2.

Table 2-2
VRV02-BA/BB Set-Up

Model	50/60Hz	Interlace/Non-Interlace
VSV11-AP VS11-AP	60Hz (4 xxx0)	Non-Interlace (3 xxx0)
VSV11-AR VS11-AR	50Hz (4 xxx1)	Non-Interlace (3 xxx0)
VSV11-AS VS11-AS	60Hz (4 xxx0)	Interlace (3 xxx1)
VSV11-AT VS11-AT	50Hz (4 xxx1)	Interlace (3 xxx1)

12. When all SETUP parameters have been selected, press the "SHIFT" and "S" keys simultaneously (while still in SETUP mode) to store the parameters.

13. Leave the monitor ON to allow for the 30-minute warm-up time required for accurate graphic displays.

14. Proceed to Paragraph B.

B. Module Setup/Verification

The logic modules used in the VSV11 or VS11 are prepared for installation as follows:

B.1 M7064 Display Processor Module

The M7064 is the VSV11/VS11 interface to the host computer's bus. As such, it contains a set of four device registers and can generate four consecutive interrupt vectors. The address of the set of device registers is selected by configuring the switches on DIP-Switch pack E31; the address of the set of interrupt vectors is selected by configuring the switches on DIP-Switch pack E43. Figures 2-3 and 2-4 illustrate the selection of the Device Address and Vector, respectively. Figure 2-5 illustrates the M7064 module, showing the locations of the DIP-Switch packs.

Refer to the Considerations given in Paragraph 2.2 to assign the Device Address and Interrupt vector.

Figures 2-3 through 2-5 give the switch settings for a Device Address (DPC) of 772010 and an Interrupt Vector Address of 320.

NOTE

If the switches are of the "rocker" type, a switch is OFF if it is pushed in at the bottom (red line showing on top); it is ON if it is pushed in at the top.

When the assignments have been made, record the information for future reference.

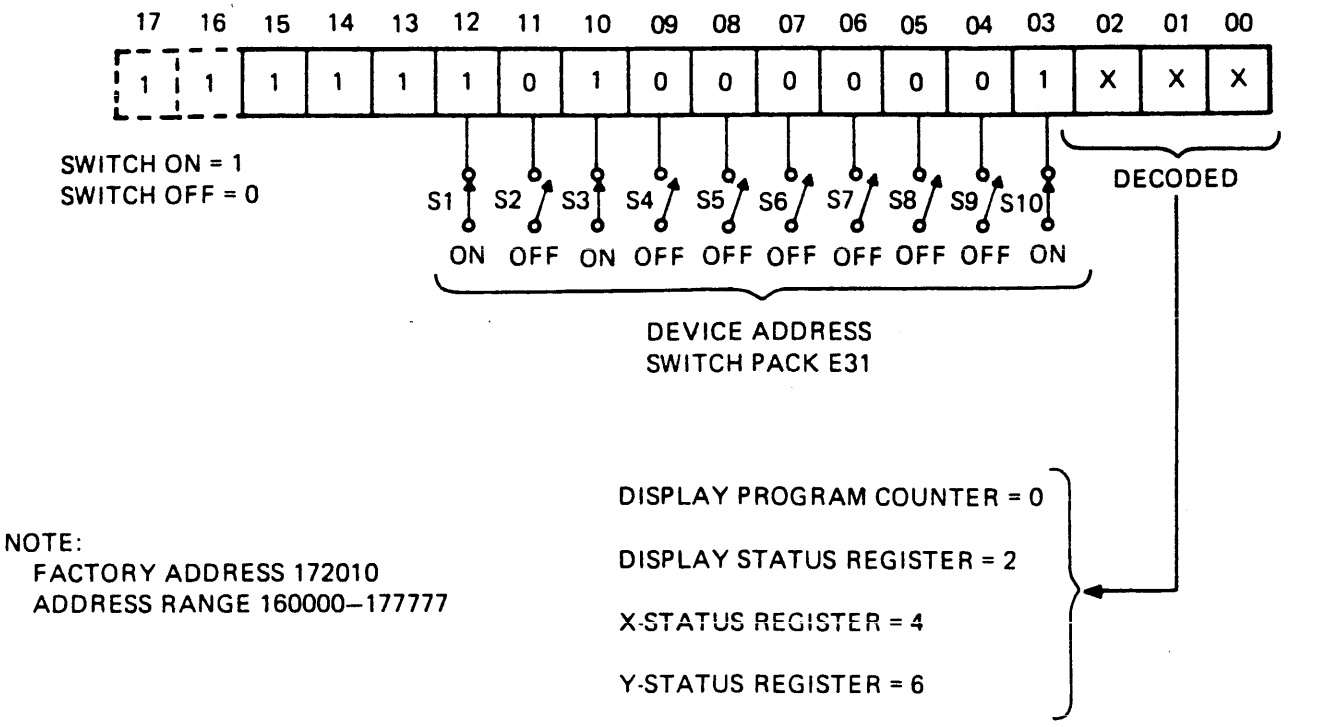


Figure 2-3
Device Address Selection

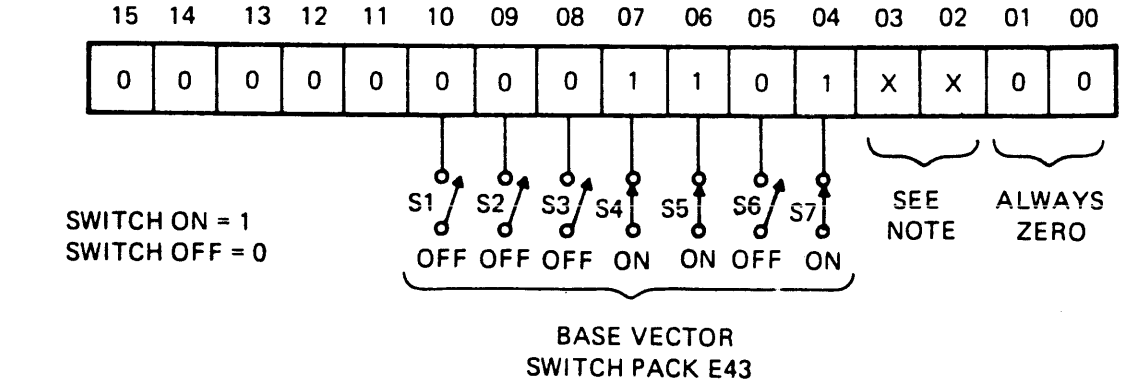


Figure 2-4
Vector Address Selection

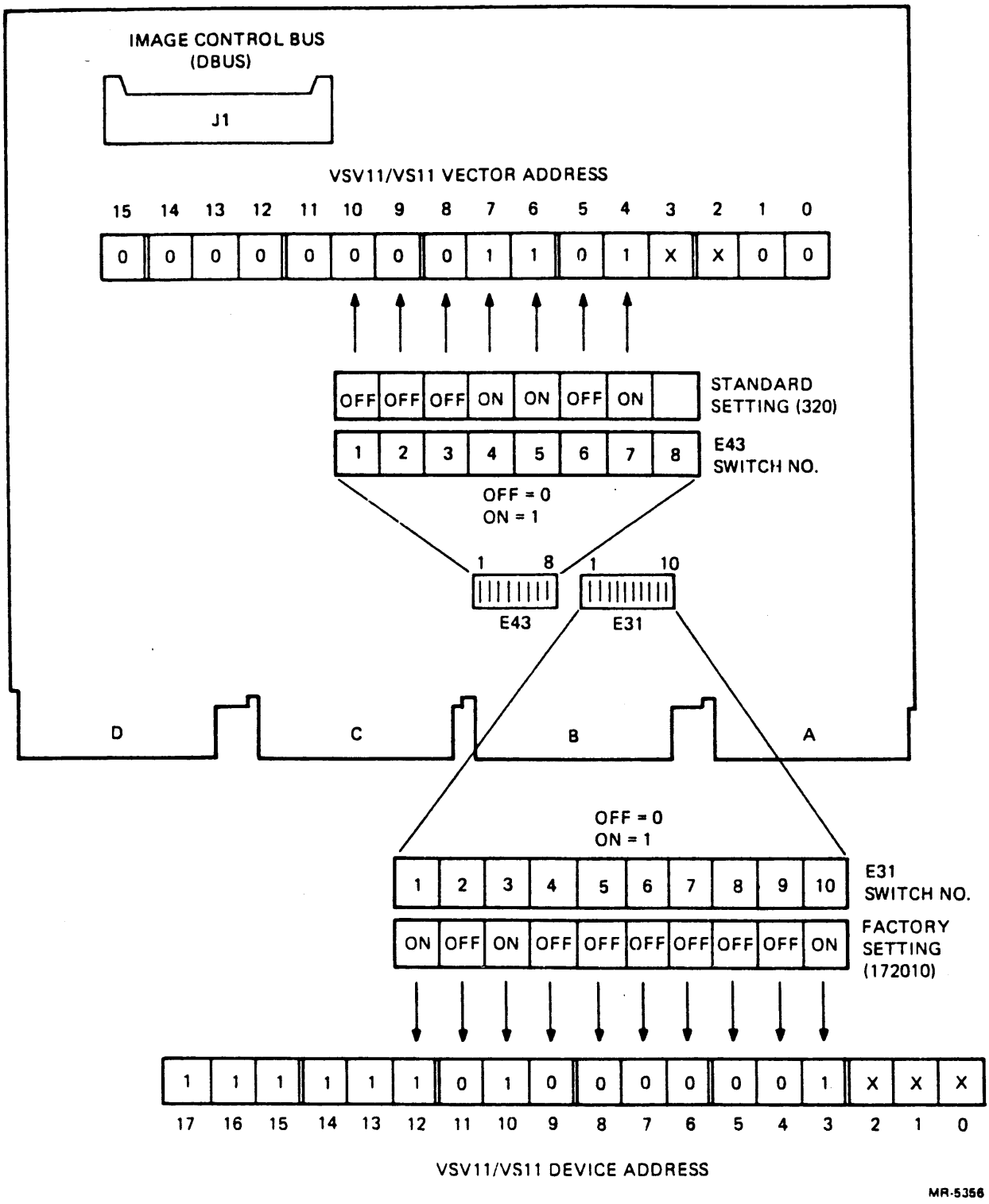


Figure 2-5
M7064 Display Processor Module

B.2 M7062 Image Memory Module(s)

Image Memory setup depends upon the model of VSV11 or VS11 being installed, depending upon whether one or two M7062 modules are present. If one module is used, it is set up for 4 bits, Non-Interlaced. If two are used, the setup is for 4 bits, operating in the Interlaced mode, with each module handling two bits.

If the unit contains one M7062 module (VSV11/VS11-AA, -AB, -AE, -AF, -AP, -AR), refer to Figure 2-6 and configure the switches on DIP-Switch packs E59 and E49 according to Table 2-3.

NOTE

If the switches are of the "rocker" type, a switch is OFF if it is pushed in at the bottom (red line showing on top); it is ON if it is pushed in at the top.

Table 2-3
M7062 Switch Settings (Single Memory)

Switch No.	E59	E49
1	OFF	OFF
2	OFF	OFF
3	ON	ON
4	ON	ON
5	ON	ON
6	ON	ON
7	OFF	OFF
8	OFF	OFF
9	OFF	OFF
10	OFF	OFF

Note, as a double check, that the switches on E59 and E49 are set identically.

On all M7062 modules, regardless of VSV11/VS11 model, verify the following jumpers:

W1, W2, W5, and W6 Installed
W3 and W4 Removed

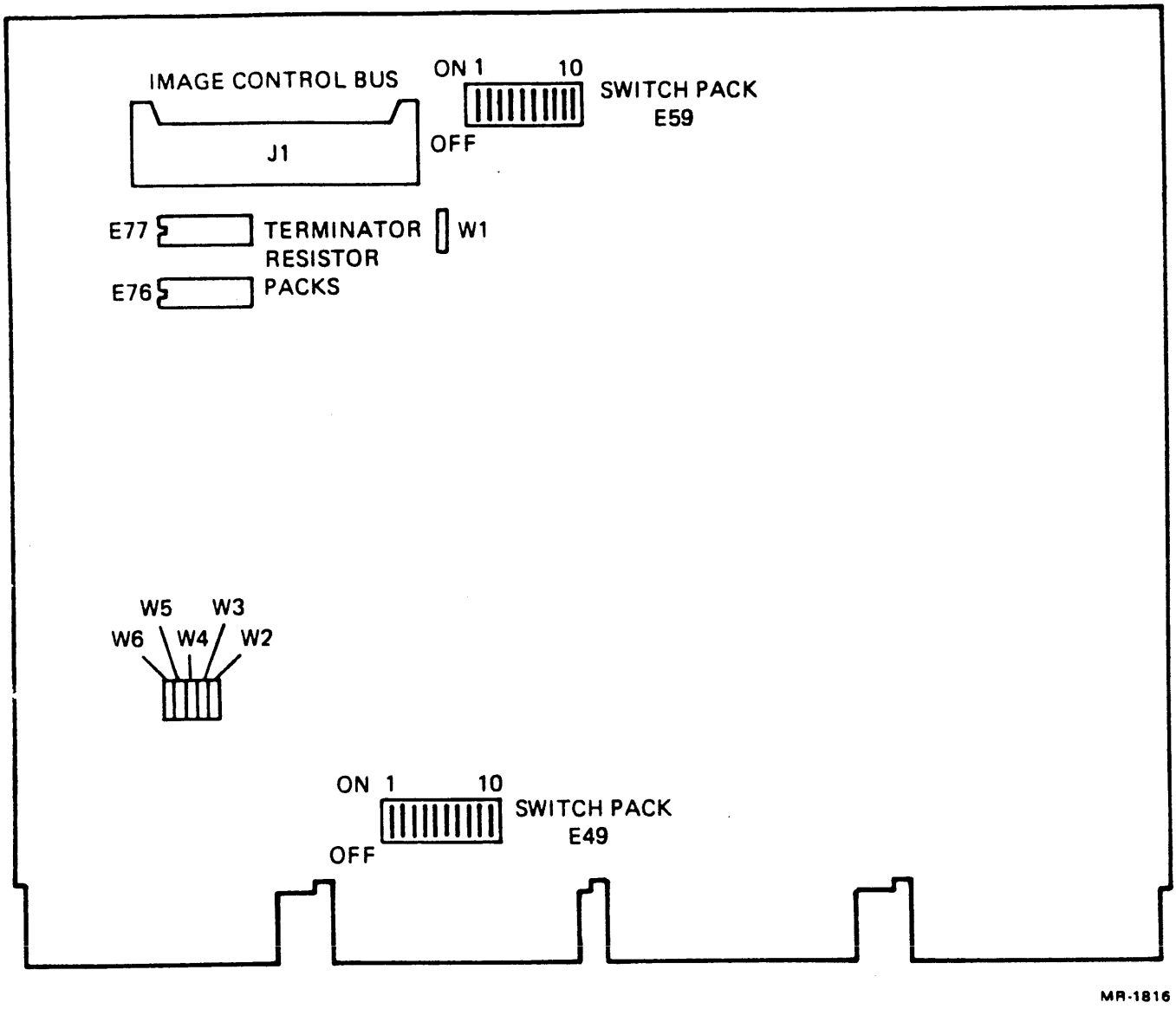


Figure 2-6
M7062 Image Memory Module

If the unit contains <u>two</u> M7062 modules (VSV11/VS11-AC, -AD, -AH, -AJ, -AS, -AT), verify that resistor packs are installed on at least one of the M7062 modules at IC locations E76 and E77. If both modules have resistor packs installed, take one of the modules with the packs installed and designate this the "first" M7062 Image Memory ("Module 1"). Remove the resistor packs from E76 and E77 on the other M7062 and designate this the "second" M7062 ("Module 2"). Refer to Figure 2-6 and configure the switches on DIP-switch packs E59 and E49 on the modules according to Table 2-4.

NOTE

If the switches are of the "rocker" type, a switch is OFF if it is pushed in at the bottom (red line showing on top); it is ON if it is pushed in at the top.

Table 2-4
M7062 Switch Settings (Dual Memory)

	Module 1		Module 2	
Switch No.	E59	E49	E59	E49
1	ON	ON	ON	ON
2	ON	ON	ON	ON
3	ON	ON	OFF	OFF
4	ON	ON	OFF	OFF
5	OFF	OFF	ON	ON
6	OFF	OFF	ON	ON
7	OFF	OFF	OFF	OFF
8	OFF	OFF	OFF	OFF
9	OFF	OFF	OFF	OFF
10	OFF	OFF	OFF	OFF

Note that within a single module, the switches on E59 and E49 should be set identically.

On all M7062 modules, regardless of VSV11/VS11 model, verify the following jumpers:

W1, W2, W5, and W6 Installed
W3 and W4 Removed

B.3 M7061 Sync Generator Module

Setup of the switches and jumpers on the M7061 depends on the specific VSV11 or VS11 model at hand; setup is directly related to whether one M7062 Image Memory module is being used or two M7062 Image Memory modules are being used, whether a Display Monitor (VT100-LA/LB or VRV02-BA/BB) is supplied with the system, and whether the ac power frequency is 60Hz or 50Hz.

Figure 2-7 illustrates the locations of the DIP-Switch pack (E21) and the various jumpers. There are eight tables presented below, listing the switch and jumper settings for each VSV11 and VS11 model as follows:

Table 2-5:	VSV11-AA,	VS11-AA		
Table 2-6:	VSV11-AB,	VS11-AB		
Table 2-7:	VSV11-AC,	VS11-AC		
Table 2-8:	VSV11-AD,	VS11-AD		
Table 2-9:	VSV11-AE,	VS11-AE,	VSV11-AP,	VS11-AP
Table 2-10:	VSV11-AF,	VS11-AF,	VSV11-AR,	VS11-AR
Table 2-11:	VSV11-AH,	VS11-AH,	VSV11-AS,	VS11-AS
Table 2-12:	VSV11-AJ,	VS11-AJ,	VSV11-AT,	VS11-AT

Determine the model number of the unit being installed and proceed to the appropriate table; refer to Figure 2-7 and set the switches and jumpers as specified. After all switches and jumpers have been configured and verified, proceed to step B.4

Note that models without a supplied monitor (VSV11/VS11-AA, -AB, -AC, and -AD) are set up for Internal Sync, while all other models are set up for External Sync. Furthermore, models with one M7062 Image Memory module are set up for Non-Interlaced mode, while models with two M7062 Image Memory modules are set up for Non-Interlaced mode.

NOTE

If the switches are of the "rocker" type, a switch is OFF if it is pushed in at the bottom (red line showing on top); it is ON if it is pushed in at the top.

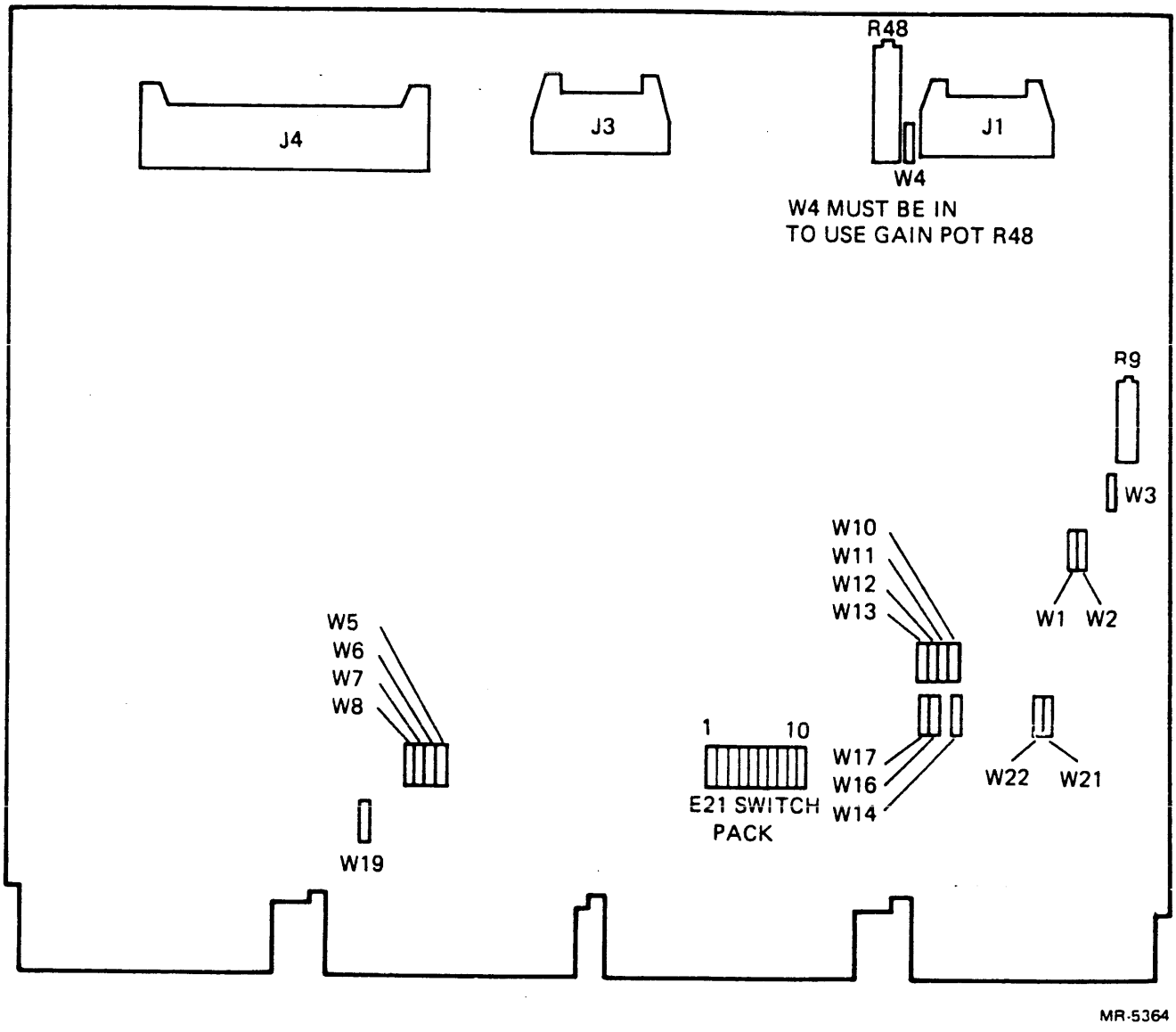


Figure 2-7
M7061 Sync Generator Module

Table 2-5
M7061 Switch & Jumper Setup for VSV11/VS11-AA
[60Hz Systems w/ One (1) M7062 Image Memory and
No Supplied Monitor]

E21 Switch No.	Setting	Jumper No.	State
1	OFF	W1	OUT
2	ON	W2	IN
		W3	OUT
3	ON	W4	IN
4	OFF	W5	OUT
5	ON	W6	IN
		W7	OUT
6	ON	W8	IN
7	OFF	W10	IN
8	ON	W11	IN
9	ON	W12	IN
10	ON	W13	IN
		W14	IN
		W16	IN
		W17	IN
		W19	IN
		W21	OUT
		W22	IN

NOTE: Jumpers W9, W15, W18, and W20 do not exist.

Table 2-6
M7061 Switch & Jumper Setup for VSV11/VS11-AB
[50Hz Systems w/ One (1) M7062 Image Memory and
No Supplied Monitor]

E21 Switch No.	Setting	Jumper No.	State
1	ON	W1	OUT
2	OFF	W2	IN
		W3	OUT
3	ON	W4	IN
4	OFF	W5	OUT
5	ON	W6	IN
		W7	OUT
6	ON	W8	IN
7	OFF	W10	IN
8	ON	W11	IN
9	ON	W12	IN
10	ON	W13	IN
		W14	IN
		W16	IN
		W17	IN
		W19	IN
		W21	OUT
		W22	IN

NOTE: Jumpers W9, W15, W18, and W20 do not exist.

Table 2-7
M7061 Switch & Jumper Setup for VSV11/VS11-AC
[60Hz Systems w/ Two (2) M7062 Image Memories and
No Supplied Monitor]

E21 Switch No.	Setting	Jumper No.	State
1	OFF	W1	OUT
2	ON	W2	IN
		W3	OUT
3	OFF	W4	IN
4	OFF	W5	OUT
5	ON	W6	IN
		W7	OUT
6	ON	W8	IN
7	OFF	W10	IN
8	ON	W11	IN
9	ON	W12	IN
10	ON	W13	IN
		W14	IN
		W16	IN
		W17	IN
		W19	IN
		W21	OUT
		W22	IN

NOTE: Jumpers W9, W15, W18, and W20 do not exist.

Table 2-8
M7061 Switch & Jumper Setup for VSV11/VS11-AD
[50Hz Systems w/ Two (2) M7062 Image Memories and
No Supplied Monitor]

E21 Switch No.	Setting	Jumper No.	State
1	ON	W1	OUT
2	OFF	W2	IN
		W3	OUT
3	OFF	W4	IN
4	OFF	W5	OUT
5	ON	W6	IN
		W7	OUT
6	ON	W8	IN
7	OFF	W10	IN
8	ON	W11	IN
9	ON	W12	IN
10	ON	W13	IN
		W14	IN
		W16	IN
		W17	IN
		W19	IN
		W21	OUT
		W22	IN

NOTE: Jumpers W9, W15, W18, and W20 do not exist.

Table 2-9
M7061 Switch & Jumper Setup for VSV11/VS11-AE, -AP
[60Hz Systems w/ One (1) M7062 Image Memory and
Supplied Monitor (VT100-LA or VRV02-BA)]

E21 Switch No.	Setting	Jumper No.	State
1	OFF	W1	OUT
2	ON	W2	IN
		W3	IN
3	ON	W4	IN
4	OFF	W5	OUT
5	ON	W6	IN
		W7	OUT
6	ON	W8	IN
7	ON	W10	IN
8	OFF	W11	IN
9	ON	W12	IN
10	OFF	W13	IN
		W14	IN
		W16	IN
		W17	IN
		W19	IN
		W21	OUT
		W22	IN

NOTE: Jumpers W9, W15, W18, and W20 do not exist.

Table 2-10
M7061 Switch & Jumper Setup for VSV11/VS11-AF, -AR
[50Hz Systems w/ One (1) M7062 Image Memory and
Supplied Monitor (VT100-LB or VRV02-BB)]

E21 Switch No.	Setting	Jumper No.	State
1	ON	W1	OUT
2	OFF	W2	IN
		W3	IN
3	ON	W4	IN
4	OFF	W5	OUT
5	ON	W6	IN
		W7	OUT
6	ON	W8	IN
7	ON	W10	IN
8	OFF	W11	IN
9	ON	W12	IN
10	OFF	W13	IN
		W14	IN
		W16	IN
		W17	IN
		W19	IN
		W21	OUT
		W22	IN

NOTE: Jumpers W9, W15, W18, and W20 do not exist.

Table 2-11
M7061 Switch & Jumper Setup for VSV11/VS11-AH, -AS
[60Hz Systems w/ Two (2) M7062 Image Memories and
Supplied Monitor (VT100-LA or VRV02-BA)]

E21 Switch No.	Setting	Jumper No.	State
1	OFF	W1	OUT
2	ON	W2	IN
		W3	IN
3	OFF	W4	IN
4	OFF	W5	OUT
5	ON	W6	IN
		W7	OUT
6	ON	W8	IN
7	ON	W10	IN
8	OFF	W11	IN
9	ON	W12	IN
10	OFF	W13	IN
		W14	IN
		W16	IN
		W17	IN
		W19	IN
		W21	OUT
		W22	IN

NOTE: Jumpers W9, W15, W18, and W20 do not exist.

Table 2-12
M7061 Switch & Jumper Setup for VSV11/VS11-AJ, -AT
[50Hz Systems w/ Two (2) M7062 Image Memories and
Supplied Monitor (VT100-LB or VRV02-BB)]

E21 Switch No.	Setting	Jumper No.	State
1	ON	W1	OUT
2	OFF	W2	IN
		W3	IN
3	OFF	W4	IN
4	OFF	W5	OUT
5	ON	W6	IN
		W7	OUT
6	ON	W8	IN
7	ON	W10	IN
8	OFF	W11	IN
9	ON	W12	IN
10	OFF	W13	IN
		W14	IN
		W16	IN
		W17	IN
		W19	IN
		W21	OUT
		W22	IN

NOTE: Jumpers W9, W15, W18, and W20 do not exist.

B.4 M8217 UNIBUS to LSI-11 Bus Converter Module (VS11 Only)

The M8217 contains a Bus-Grant Jumper Plug. If the BR level on the plug does not correspond to the desired VS11 BR level, remove the plug and install one of the desired level.

2.4 OPTION INSTALLATION

A. At this point, take the time to familiarize yourself with the VSV11 and VS11 Field Maintenance Print Set shipped with the unit. Specifically, inspect the following drawings:

C-IC-VSV11-0-4 (Interconnection Diagram)
D-UA-VSV11-0-0 (Unit Assembly)
D-UA-VS11-0-0 (Unit Assembly)

In addition, if the unit is a VS11, become familiar with Figures 2-8 through 2-12 in this section depicting the mounting of the DDV11-CK backplane in various types of mounting boxes. The DW11 Installation Guide, EK-DW11A-IN, can also be consulted if desired.

B. If the unit being installed is a VS11, perform the following steps:

1. Mount the DDV11-CK in the designated mounting box (refer to Figures 2-8 through 2-11 for the type of box at hand). Although not illustrated, installation of the DDV11-CK into a BA11-A box is similar to that for the BA11-K.

2. Connect the power harness to the nearest outlet on the mounting box dc power distribution block. If the box is a BA11-F or BA11-P, use the Power Harness Adapter Cable (#70-16830) as an extension in order to reach the block.

3. Test for shorts between the following backplane Power and Ground pins:

A2 (Any slot) = +5V
C2, T1 (Any slot) = GROUND
S1 (Slot 1, Rows A or B) = +15V
D2 (Any slot, Rows A thru D) = +12V
U2 (Row E, slot 1) = -5V

4. Install a G7272 Grant Continuity Card in slots A2 and A3 of the DDV11-CK backplane (Figure 2-12).

NOTE

Make certain that the Grant Continuity Card is a G7272, for use on the LSI-11 Bus, and NOT a G727 UNIBUS Grant Continuity Card. Use of a G727 will prevent proper bus operation.

5. Locate the SPC slot on the UNIBUS designated to hold the M8217 UNIBUS to LSI-11 Bus Converter Module and remove the NPG jumper between backplane pins CA1 and CB1 (i.e., pins A1 and B1 in Row C of the UNIBUS backplane slot).

6. Refer to drawing D-UA-VS11-0-0 and connect the two BC05L-06 cables to the connectors on the M8217 module (J1 and J2).

7. Install the M8217 module into the UNIBUS SPC slot (Figure 2-12).

8. Refer to drawing D-UA-VS11-0-0 and connect the two BC05L-06 cables to the M9403 Connector Module. Note that the cable connected to the Top connector on the M8217 (J1, nearest the handle of the module) connects to the Bottom connector on the M9403 (J1, nearest the finger end of the module) and vice versa. When both modules are facing the same direction and in the same orientation, the cables should be together with no twists.

9. Install the M9403 module into slots A1-B1 of the DDV11-CK backplane (Figure 2-12).

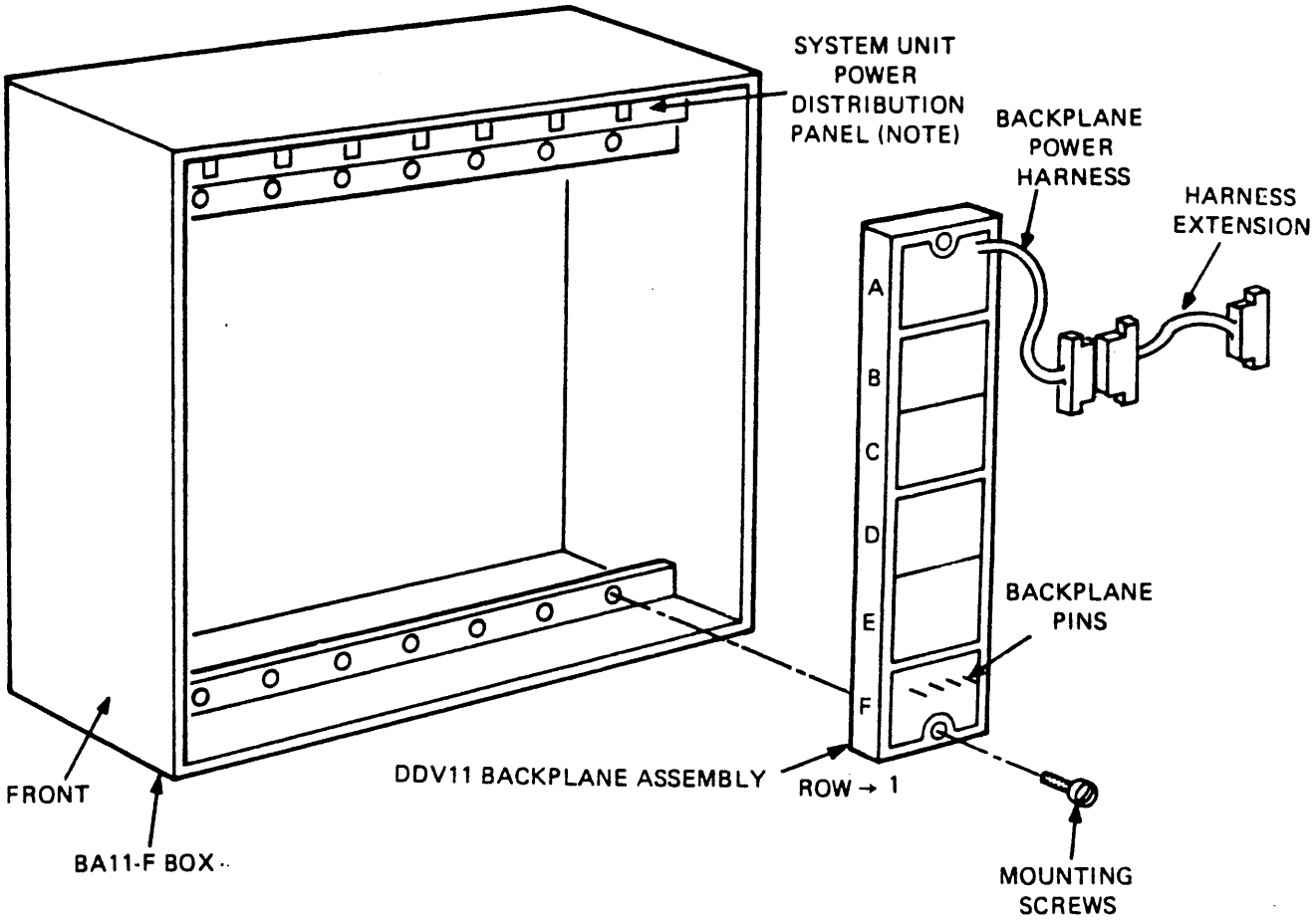
10. Turn on system power and verify that the following voltages are present on the DDV11-CK and within ±5% of their nominal values:

    +5Vdc (Pin A2, any slot)
    +15Vdc (Pin AS1, slot 1)
    +12Vdc (Pin CD2, slot 1)

    Note the level of the +12Vdc signal; if it is out of range, the regulator on the M9403 must be adjusted by turning the potentiometer near the handle of the M9403.

11. Verify that the computer system's UNIBUS is not hung (i.e., that the computer can be "booted" and run normal programs).

12. Power the system down and proceed to the next step.



NOTE:
THE DW11 OPTION CANNOT BE INSTALLED INTO PDP-11/45 PROCESSORS WITH SERIAL NUMBERS BELOW 2000 BECAUSE OF THE DIFFERENT TYPE CONNECTORS ON THE SYSTEM UNIT POWER DISTRIBUTION PANEL.

MR-0731

Figure 2-8
Installing DDV11-CK Backplane Into BA11-F Box

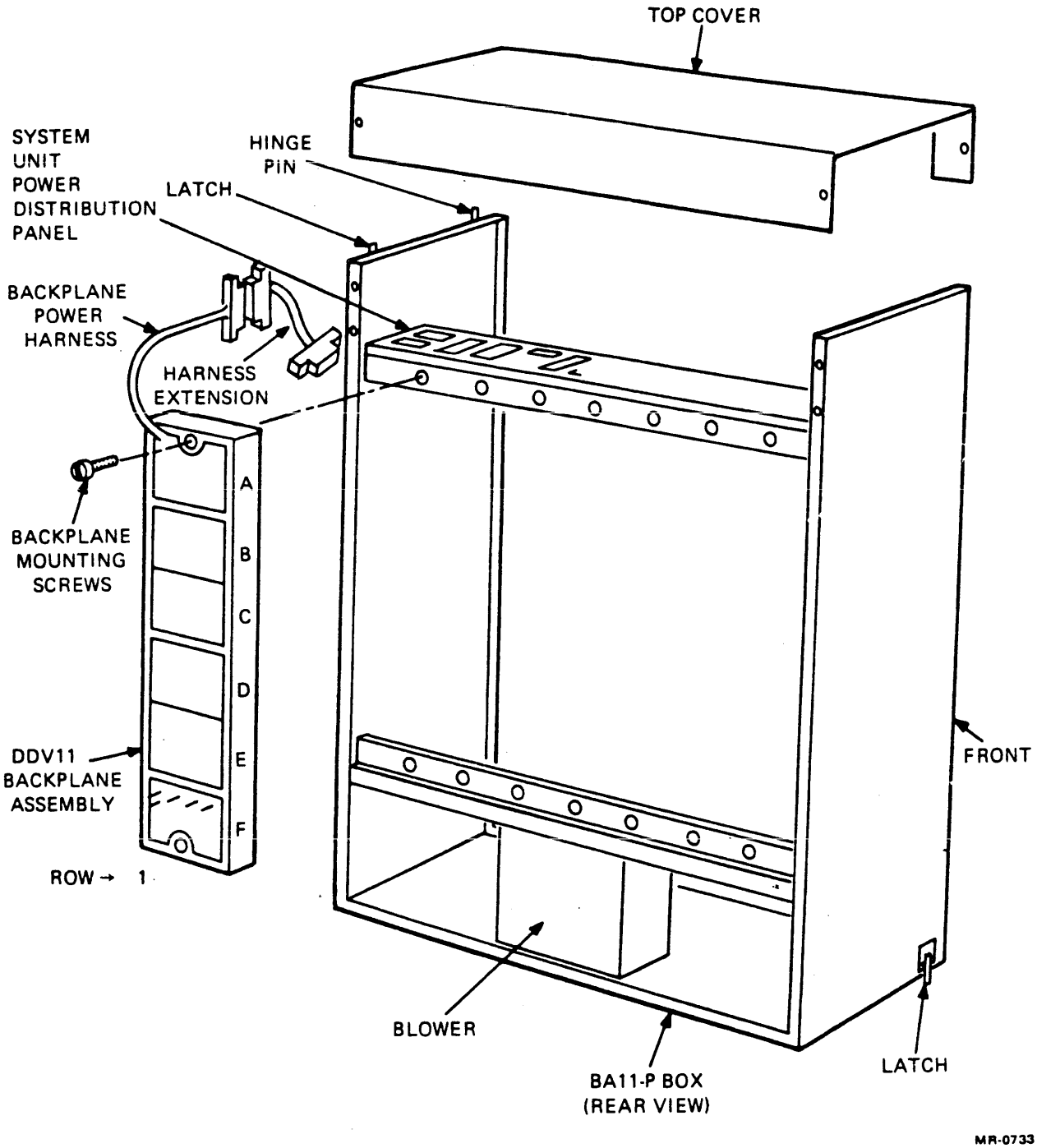


Figure 2-9
Installing DDV11-CK Backplane Into BA11-P Box

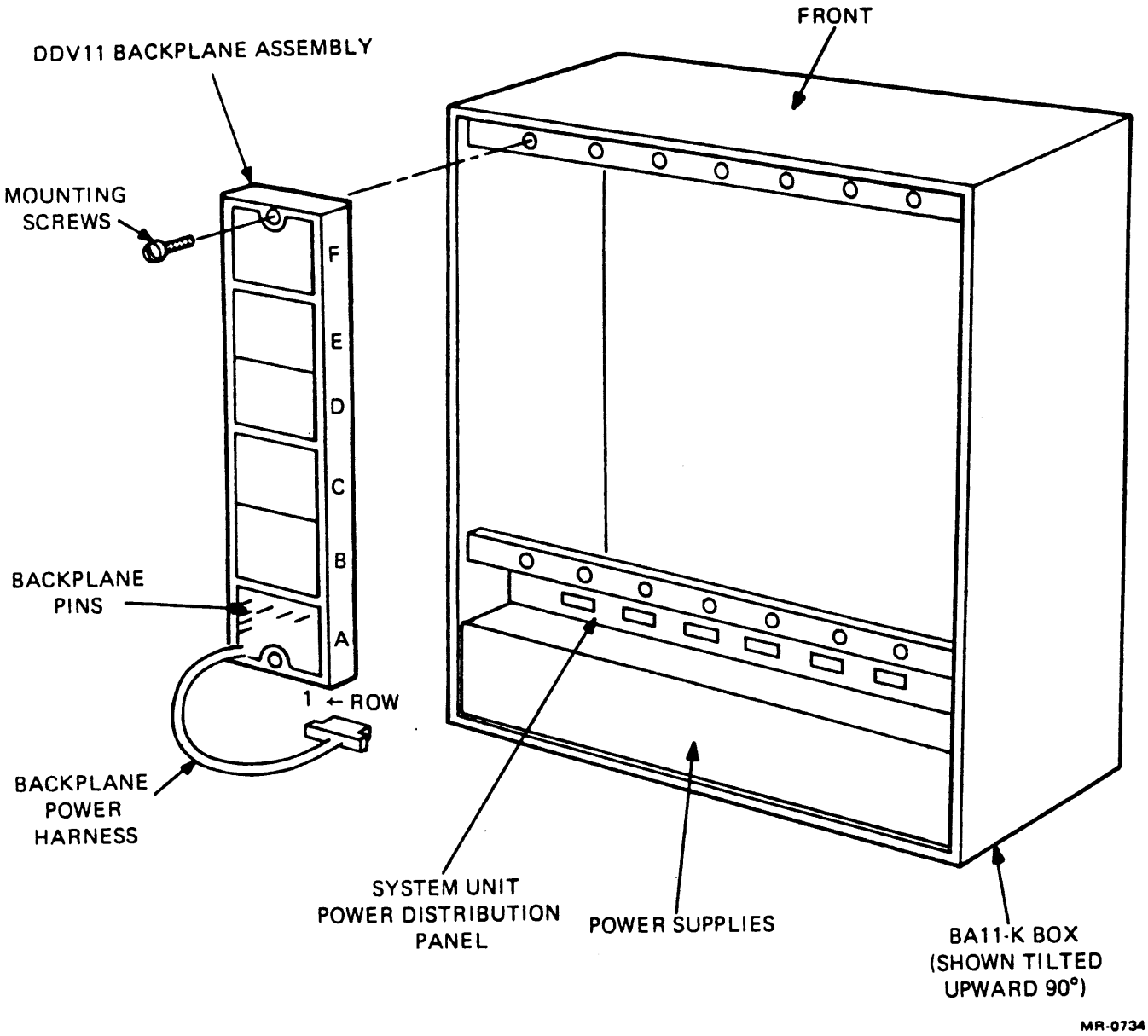
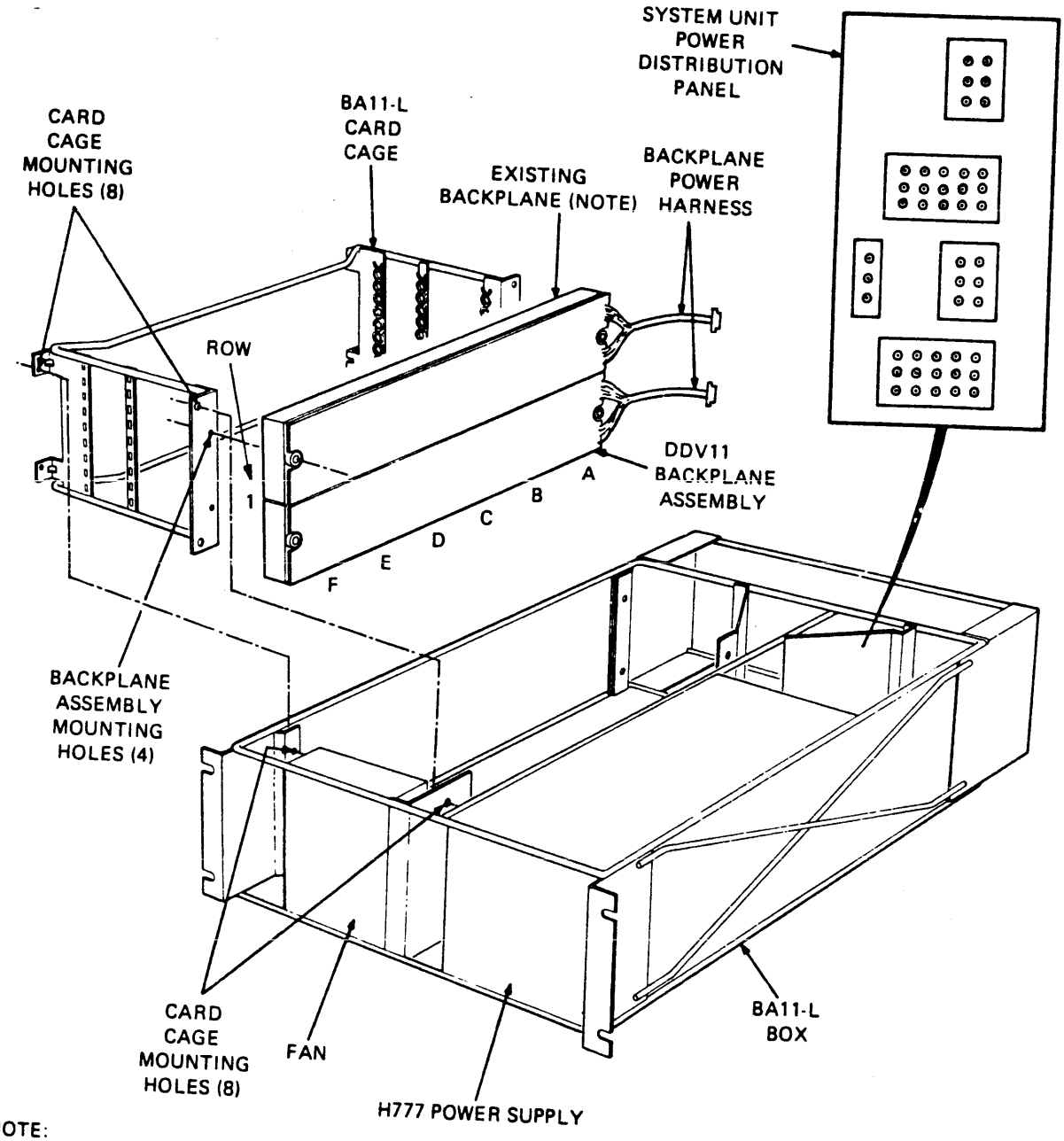
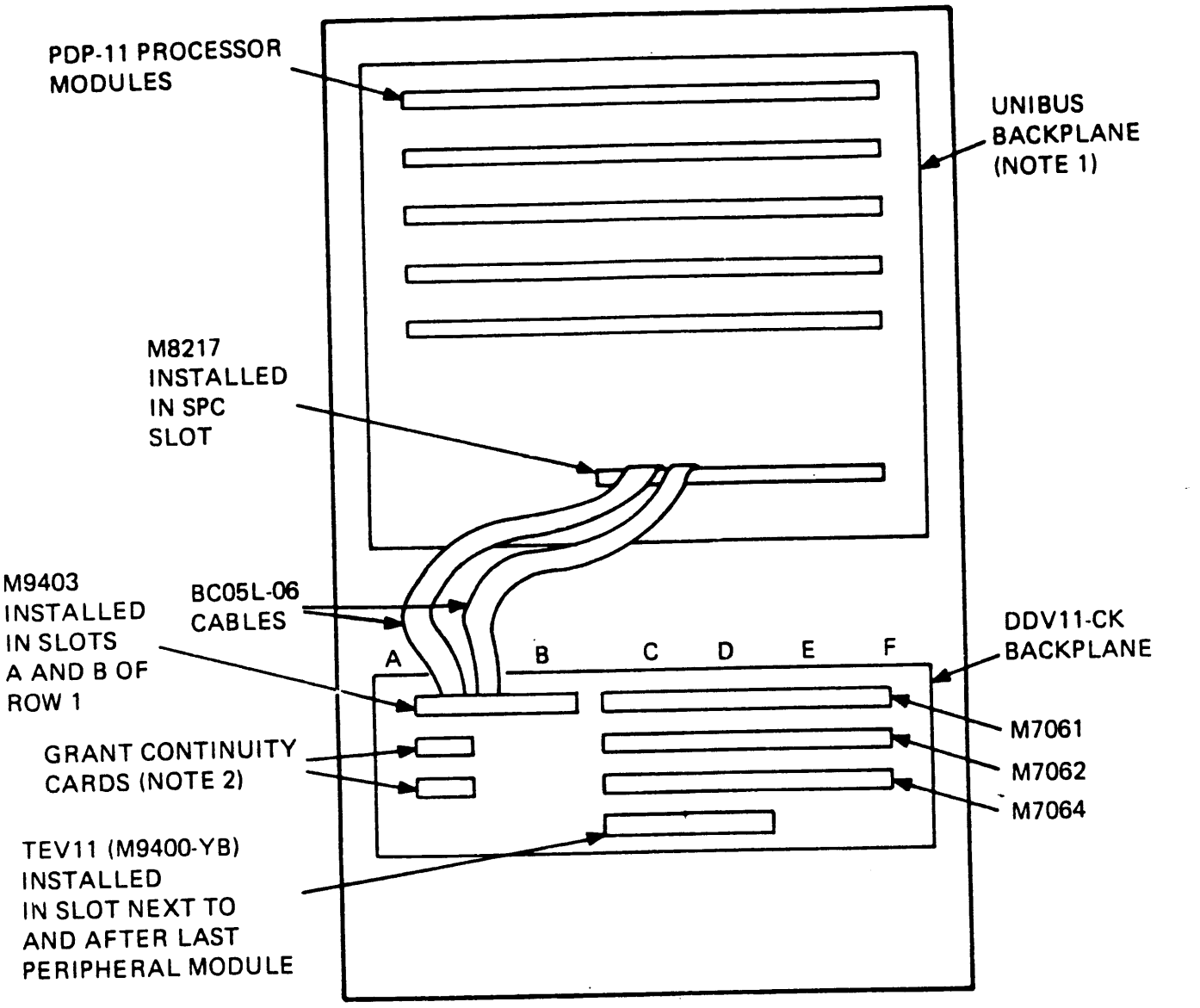


Figure 2-10
Installing DDV11-CK Backplane Into BA11-K Box



NOTE:
THE EXISTING BACKPLANE CAN OCCUPY EITHER THE UPPER OR LOWER BACK-PLANE POSITION ON THE CARD CAGE.

Figure 2-11
Installing DDV11-CK Backplane Into BA11-L Box



NOTES:

1. IF UNIBUS BACKPLANE IS A DD11-B, -C, -D, OR -P, THE BACKPLANE MUST BE AT THE PROPER REVISION LEVEL.
2. IF THESE SLOTS ARE UNUSED, G7272 GRANT CONTINUITY CARDS MUST BE INSTALLED HERE.

MR-1825

Figure 2-12
VS11 Graphic System Basic Configuration

C. Module Set Installation

The VSV11/VS11 module set (M7061, M7062, M7064) is installed in a backplane with two distinct buses: an LSI-11 Bus, and a "C-D Interconnect". If the system is a VSV11, the modules are installed in an H9273-A backplane (or equivalent), illustrated in Figure 2-13. This backplane contains nine rows, each with four slots. The A and B slots are wired according to the LSI-11 Bus Specification; the VSV11 interfaces to the host computer via these signals. The first backplane row can contain either a central processor unit or a connector extending the bus from another backplane. If the first row contains a CPU, jumpers W1 through W3 must remain installed; if the first row contains a bus connector, jumpers W2 and W3 must be removed. The connectors in slots C and D have no connections to the LSI-11 Bus. Rather, C- and D-Slot pins on side 2 of each row are connected to the C- and D-Slot pins on side 1 in the next lower row. This "C-D Interconnect" carries the Video Bus signals of the VSV11.

VS11 systems use the DDV11-CK backplane, illustrated in Figure 2-14. This backplane also provides two distinct buses: an LSI-11 Bus (slots A, B, C, and D) and a Video Bus (slots E and F, the "C-D Interconnect"). The VS11 modules must use the Video Bus, slots E and F, and therefore must connect to the LSI-11 Bus in the C and D slots. Although the A-B slots can be used for other dual-height LSI-11 Bus interface modules, it is recommended that this not be done.

Figures 2-12 and 2-15 illustrate the configuration of modules within the DDV11 backplane, while Figures 2-16 and 2-17 illustrate the configuration of modules within the H9273 backplane. Note that in all cases, the VSV11/VS11 modules must be adjacent to provide the proper interconnect.

The VSV11/VS11 module set is further interconnected via the 40-conductor DBUS Data Cable connected to each module. Figure 2-18 illustrates the arrangement of the cable and its connection to each module, and Figure 2-19 shows the DBUS connector pin assignments.

Referring to Figures 2-12 through 2-18 and Unit Assembly drawing D-UA-VSV11-0-0, install the VSV11/VS11 module set into the designated backplane (DDV11-CK for VS11, existing LSI-11-BUS backplane for VSV11) as follows:

1. Make sure system power is OFF.

2. Locate the modules (M7061, M7064, and one or two M7062) and the DBUS Data Cable (#70-15987).

3. Refer to Figure 2-18 and insert one end of the DBUS cable into the 40-pin header (J4) on the M7061 module; the red locating stripe on the cable should be near the UU-VV end of the header.

4. Insert the M7061 into its designated backplane row (in VSV11 systems, Figure 2-16 or 2-17, this row will be nearest the LSI-11 processor; in VS11 systems, Figure 2-12 or 2-15, this is Row 1, Slots C through F, of the DDV11-CK).

5. Locate the M7062 Image Memory module with resistor packs installed in locations E76 and E77 (in some VSV11/VS11 systems, this will be the only M7062). If only one M7062 is being installed, insert the second "tap" connector (of the two "tap" connectors that are on the cable) of the DBUS cable (as counted from the end inserted into the M7061) into the 40-pin header (J1) on the M7062, with the red locating stripe located nearest header pins UU-VV. If two M7062 modules are being installed, insert the first tap connector of the DBUS cable (the one nearest the M7061) into M7062 header J1.

6. Refer to Figures 2-12 and 2-15 through 2-17 and insert the M7062 into the backplane row adjacent to and "downstream" from the M7061 (i.e., the next higher-numbered row).

7. If a second M7062 Image Memory is being installed (it should have the resistor packs removed from positions E76 and E77), install the second DBUS cable connector tap into header J1 (red locating stripe near header pins UU-VV); refer to Figure 2-15 (VS11) or 2-17 (VSV11) and install the M7062 in the backplane row adjacent to the first M7062.

8. Insert the free end of the DBUS cable into 40-pin header J1 on the M7064 (with the red locating stripe on the cable nearest to header pins UU-VV) and insert the M7064 into the next backplane row. For VS11 systems, this will be row 3 in the DDV11-CK if one M7062 Image Memory was installed, (Figure 2-12) and row 4 if two M7062's were installed (Figure 2-15).

9. If the unit is a VSV11, make sure that the end of the LSI-11 Bus contains the proper terminator (in case the terminator had to be moved in order to install the VSV11) and that a G7272 Grant Continuity card is installed in any unused LSI-11 Bus backplane slots.

10. If the unit is a VS11, install the TEV11 terminator module (M9400-YA) in DDV11-CK Row 4 (Slots C-D if one M7062 was installed, Figure 2-12; or Slots A-B if two M7062's were installed, Figure 2-15). Make sure that

G7272 (not G727) Grant Continuity cards are installed in slots A2 and A3 (i.e., Row 2 slot A, and Row 3 slot A) of the DDV11-CK.

11. Verify that there is not a short circuit between +5Vdc and Ground on the backplane. Do not check for shorts on the other voltages (use of an ohmmeter could cause circuit damage if the pins are driven with the wrong polarity).

12. Proceed to Step D.

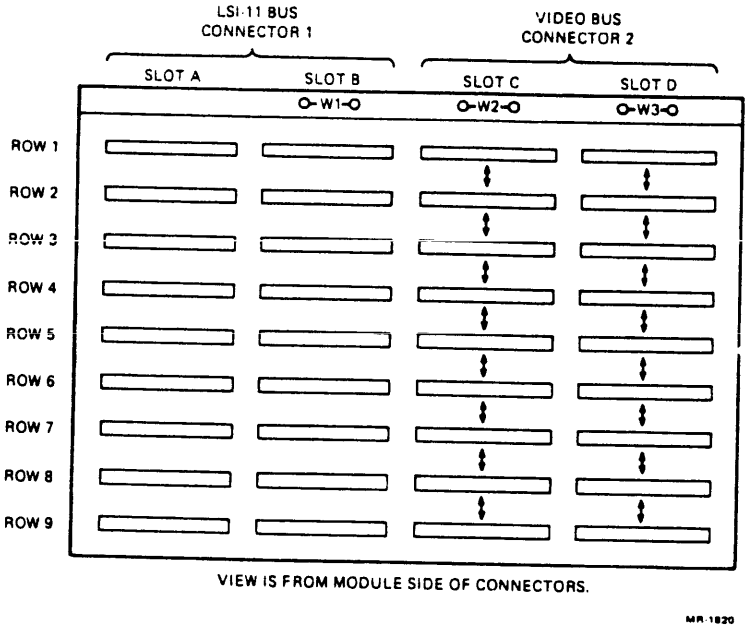


Figure 2-13
H9273-A Backplane Connectors

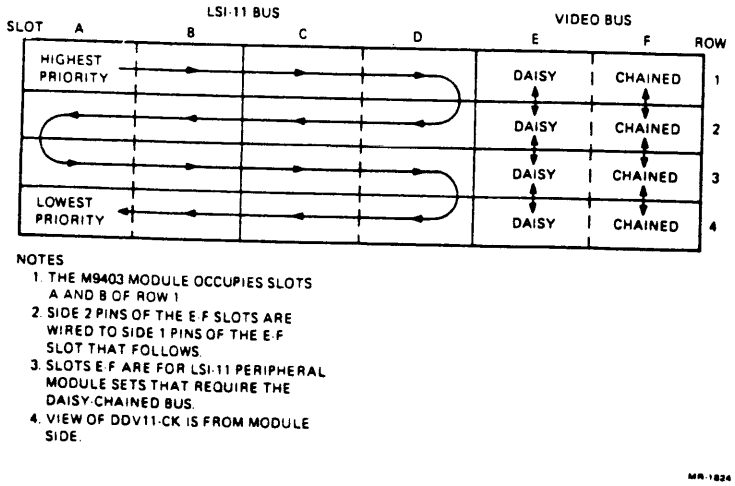
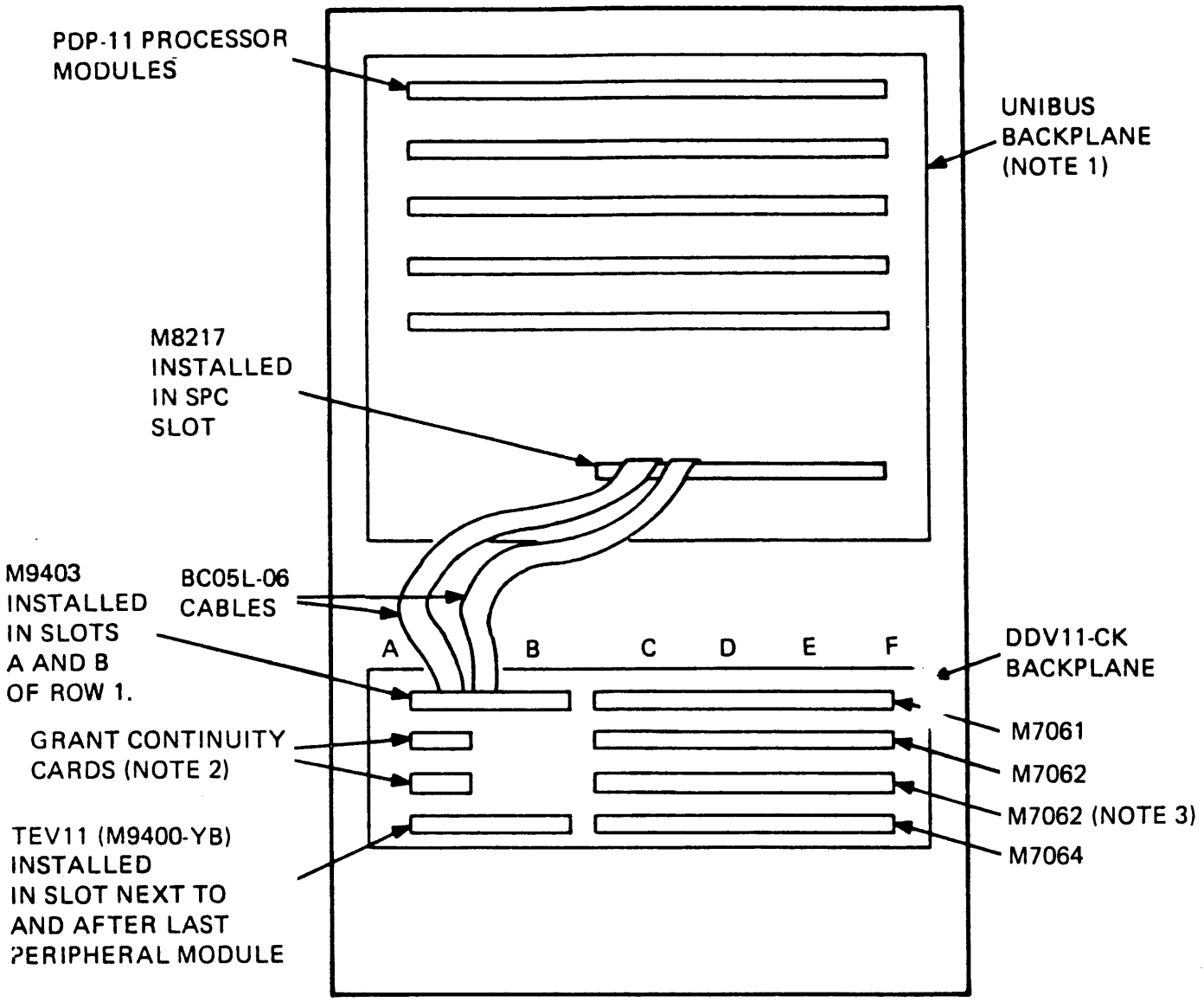


Figure 2-14
DDV11-CK Backplane Connectors



NOTES:

1. IF UNIBUS BACKPLANE IS A DD1-B, -C, -D, OR -P, THE BACKPLANE MUST BE AT THE PROPER REVISION LEVEL.
2. IF THESE SLOTS ARE UNUSED, G7272 GRANT CONTINUITY CARDS MUST BE INSTALLED HERE.
3. REMOVE THE TERMINATOR RESISTOR PACKS FROM THIS M7062.

MR-1826

Figure 2-15
VS11 Graphic System 2-Memory Configuration

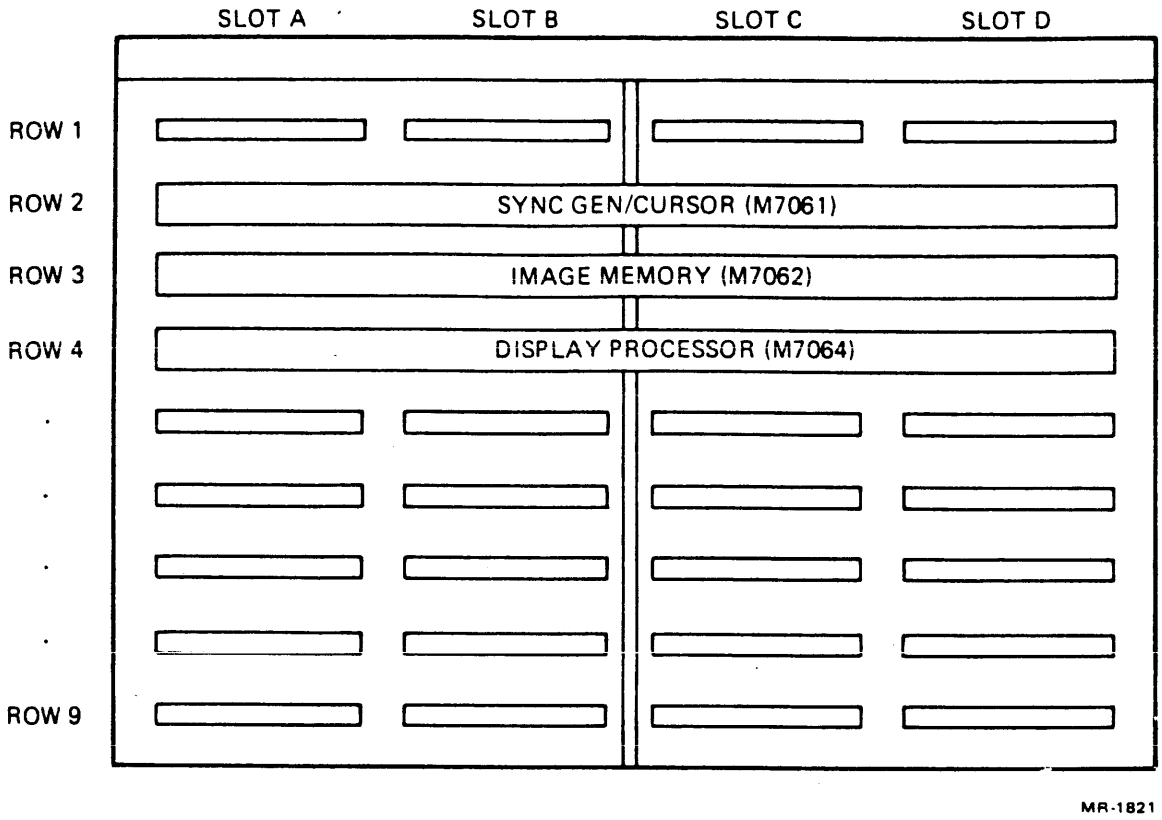


Figure 2-16
VSV11 Graphic System Basic Module Configuration

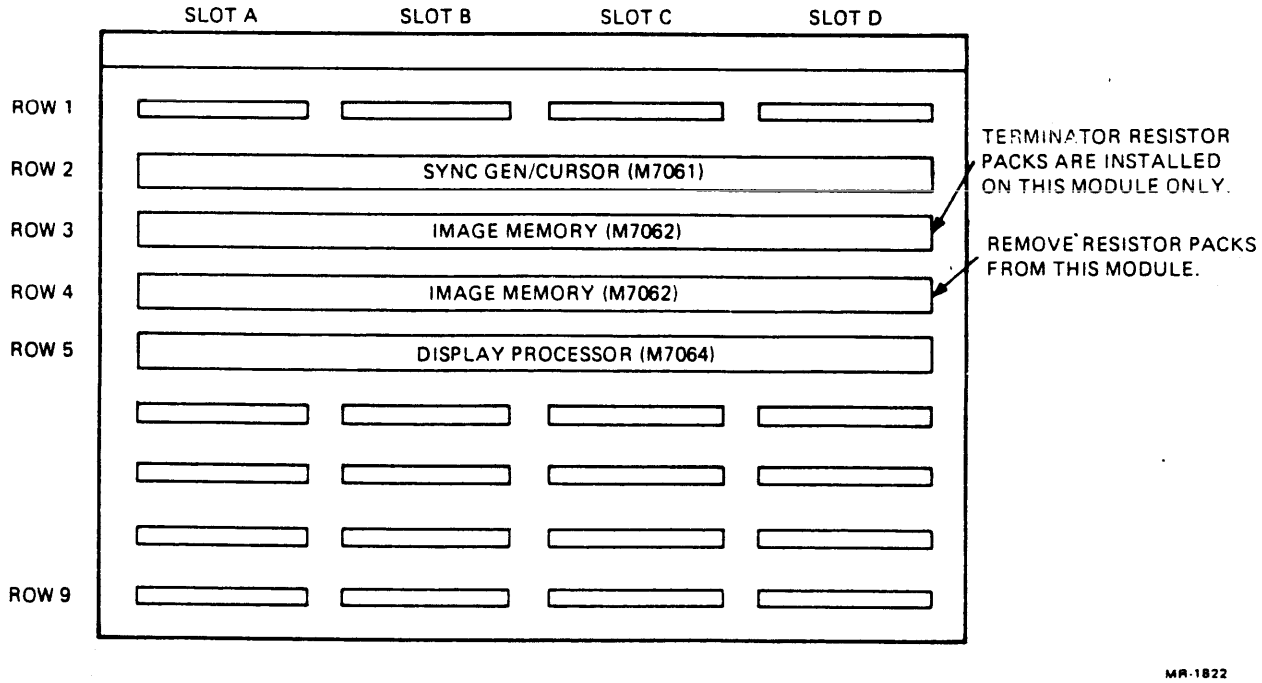


Figure 2-17
VSV11 Graphic System 2-Memory Module Configuration

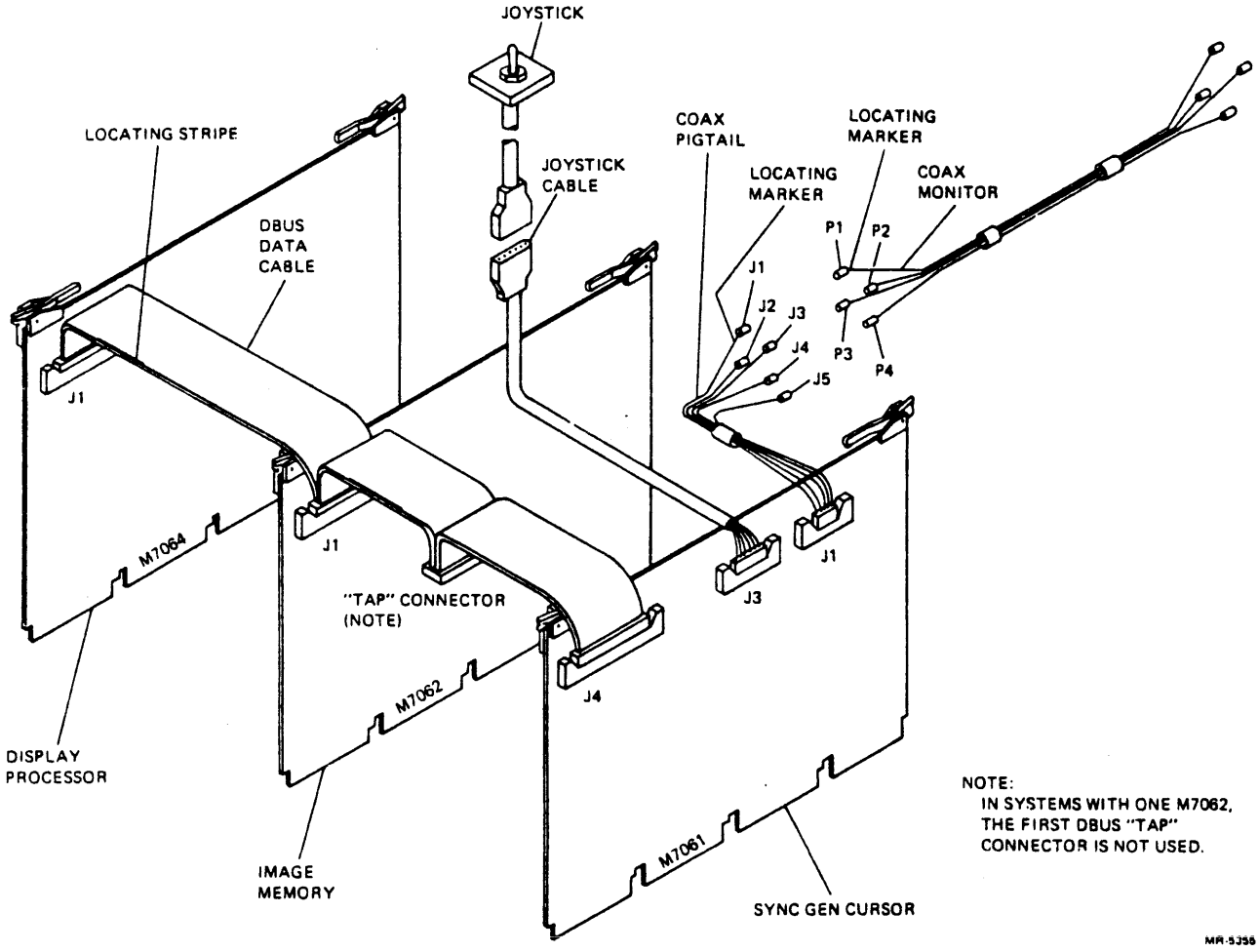


Figure 2-18
VS11/VSV11 Module Set Arrangement

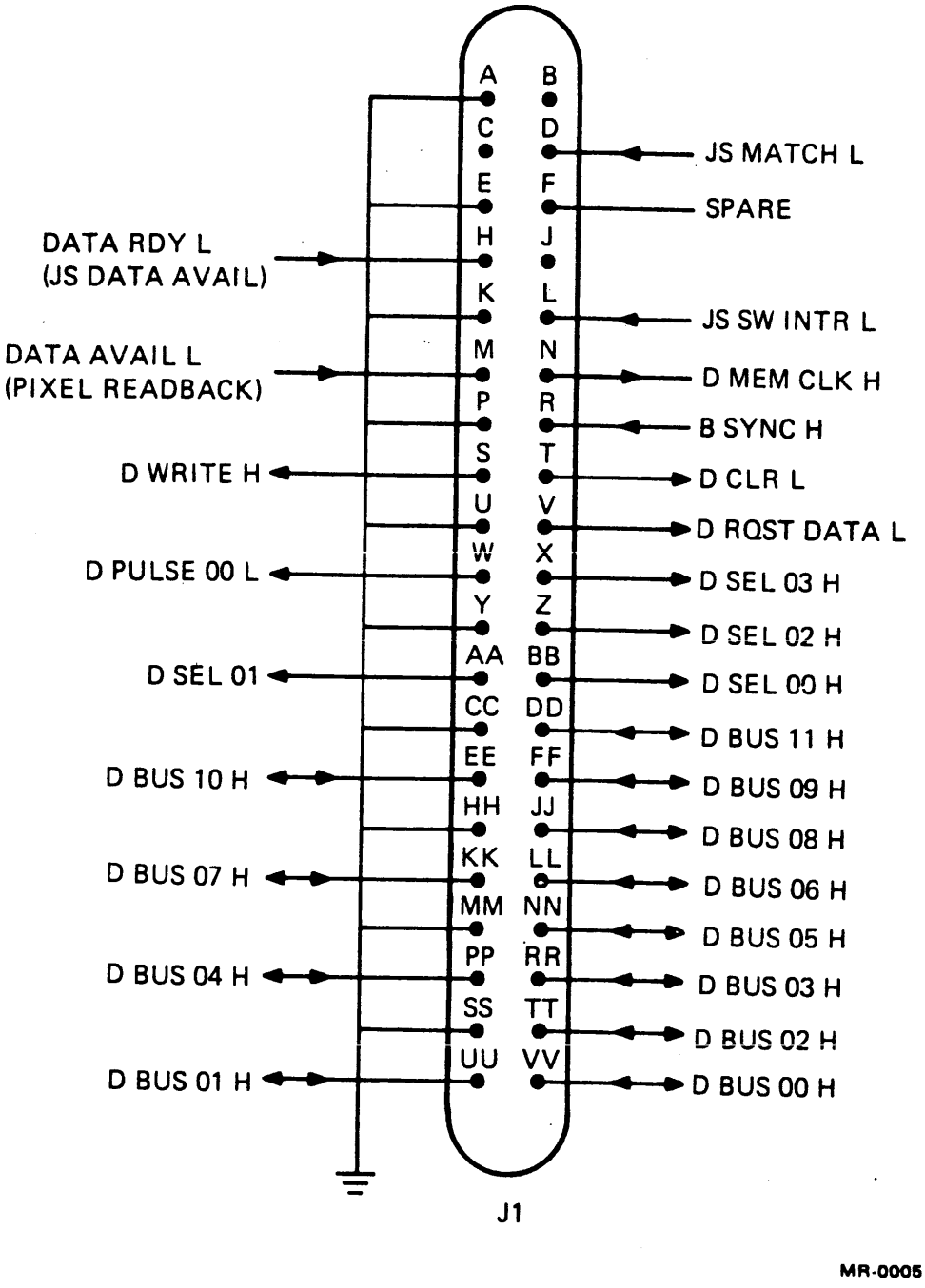


Figure 2-19
DBUS Connector Pin Assignments

D. Power up the system and verify that the following voltages are present (within a ±5% tolerance) on the backplane:

1. +5Vdc, pin A2 of any slot

2. +12Vdc, pin D2 of all slots housing the LSI-11 Bus portion of the M7061 and M7062 modules (i.e., pins AD2 and BD2 of a quad-height LSI-11 backplane; or pins CD2 and DD2 of the DDV11-CK).

3. -5Vdc, U2 of all slots housing the "Slot C" portion of the M7061 and M7062 modules (i.e., pin CU2 of a quad-height LSI-11 backplane; or pin EU2 of the DDV11-CK).

4. Verify that the host computer's bus is not hung (processor can be booted and run normal programs).

5. Proceed to Step E.

E. Monitor Connection

The video monitor is connected to the VSV11/VS11 system at connector J1 on the M7061 Sync Generator module. Figure 2-20 shows the connector signal pinning, and Figure 2-7 shows its placement on the module. To J1 is attached a 5-conductor coaxial "pigtail" cable, with an AMP connector on the module end and BNC connectors on the other end. The long 4-conductor coaxial Monitor cable, with BNC connectors at both ends, attaches to the pigtail cable. Figure 2-21 illustrates the cables. Various of the conductors are used, depending upon the type of monitor being connected.

When connecting the monitor to the system, refer to Figures 2-22 through 2-24 and to drawings D-UA-VSV11-0-0 and C-IC-VSV11-0-4, Sheets 1 and 2, in order to aid in cable and connection identification.

The procedure used for connecting the Display Monitor to the VSV11/VS11 logic depends upon the model of the unit at hand. If a Display Monitor was not supplied with the system (VSV11/VS11-AA, -AB, -AC, or -AD), proceed to Step E.1. If a VT100-LA or VT100-LB was supplied (VSV11/VS11-AE, -AF, -AH, or AJ), proceed to Step E.2. If a VRV02-BA or VRV02-BB was supplied (VSV11/VS11-AP, -AR, -AS, or -AT), proceed to Step E.3.

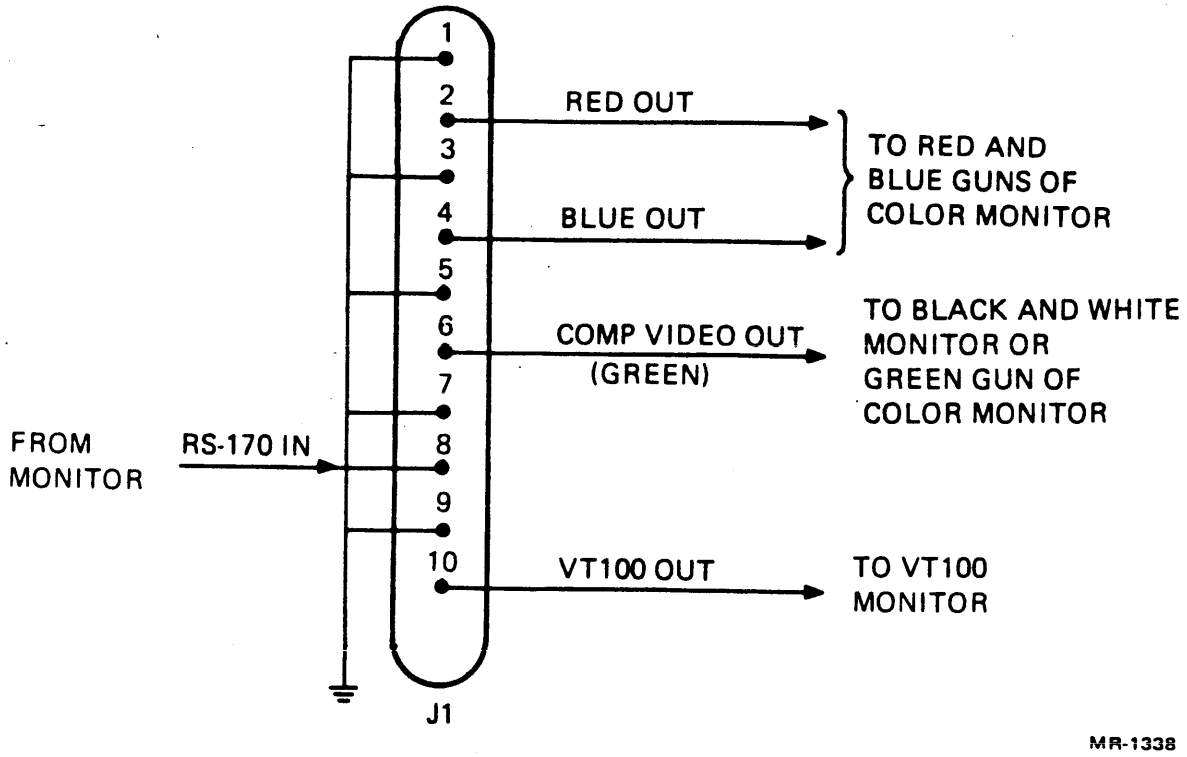


Figure 2-20
M7061 Video Connector J1 Pinning

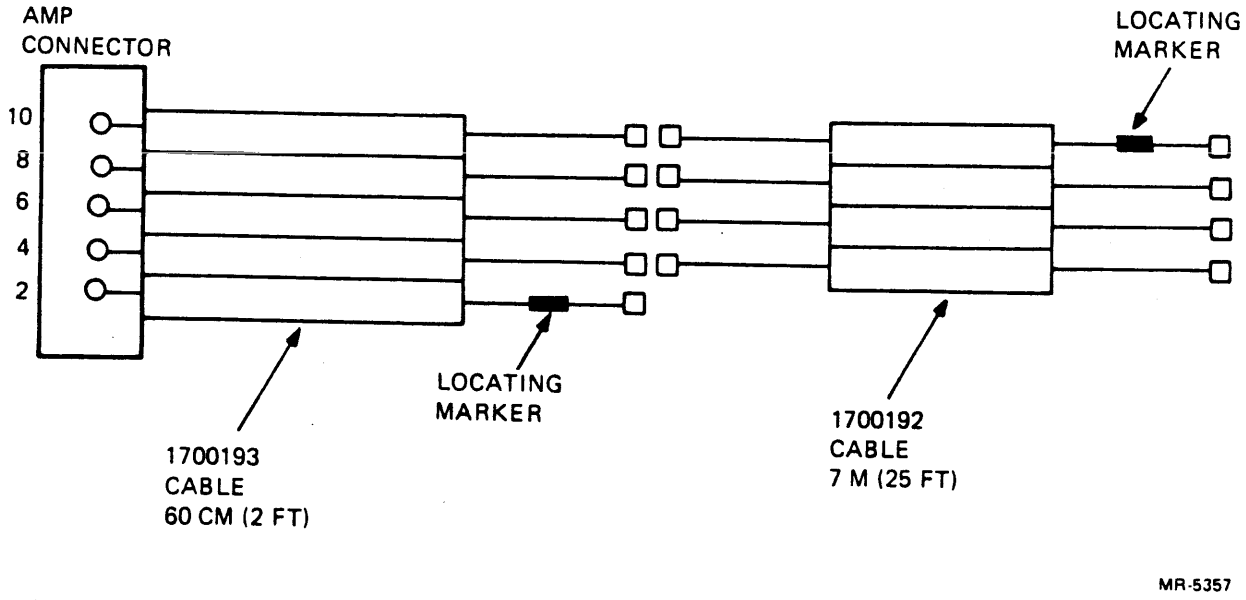


Figure 2-21
Video Cables

E. 1 Connection of Customer-Supplied Monitor -- referring to Figure 2-22, execute the following steps, then proceed to Step F.

1. Identify the 2-foot 5-Conductor coaxial pigtail cable with BNC connectors on one end and an AMP connector on the other (P/N 17-00193), and the long 4-conductor coaxial Monitor cable with BNC connectors on both ends.

2. Identify the conductor marked with the black locating marker (band) on each cable; this is conductor #1, with corresponding BNC connectors J1 and P1. Refer to drawing D-UA-VSV11-0-0 and, counting from the J1-P1 conductors, identify the J3-P3 conductors; connect J3 on the 2-foot pigtail cable to P1 on the Monitor cable.

3. The other conductors and BNC connectors of each cable are numbered in sequence from #1 when the cables are laid flat.

4. If the customer-supplied monitor is Monochrome (black and white), refer to Figure 2-22 and connect BNC connector J1 of the Monitor cable to the video input of the monitor. Alternatively, depending upon monitor type, pigtail conductor #1 (VT100-OUT) could be used for the video signal, in which case connect J1 of the pigtail cable to P1 of the Monitor cable. Then connect J1 on the other end of the Monitor cable to the video input of the monitor.

5. If the customer-supplied monitor is Color, connect J3, J4 and J5 of the pigtail cable to P1, P2 and P3, respectively, on the Monitor cable. Then connect J1, J2 and J3 at the other end of the Monitor cable to the COMPOSITE VIDEO (GREEN), BLUE, and RED inputs, respectively, of the monitor.

6. Verify that the video input(s) to the monitor are terminated in 75 ohms.

7. Observe the Key and/or "G" and "S" markings on the AMP connector on the pigtail cable. Insert the AMP connector into header J1 on the M7061 Sync Generator module, with the "G" marking nearest the the module.

8. Proceed to Step F.

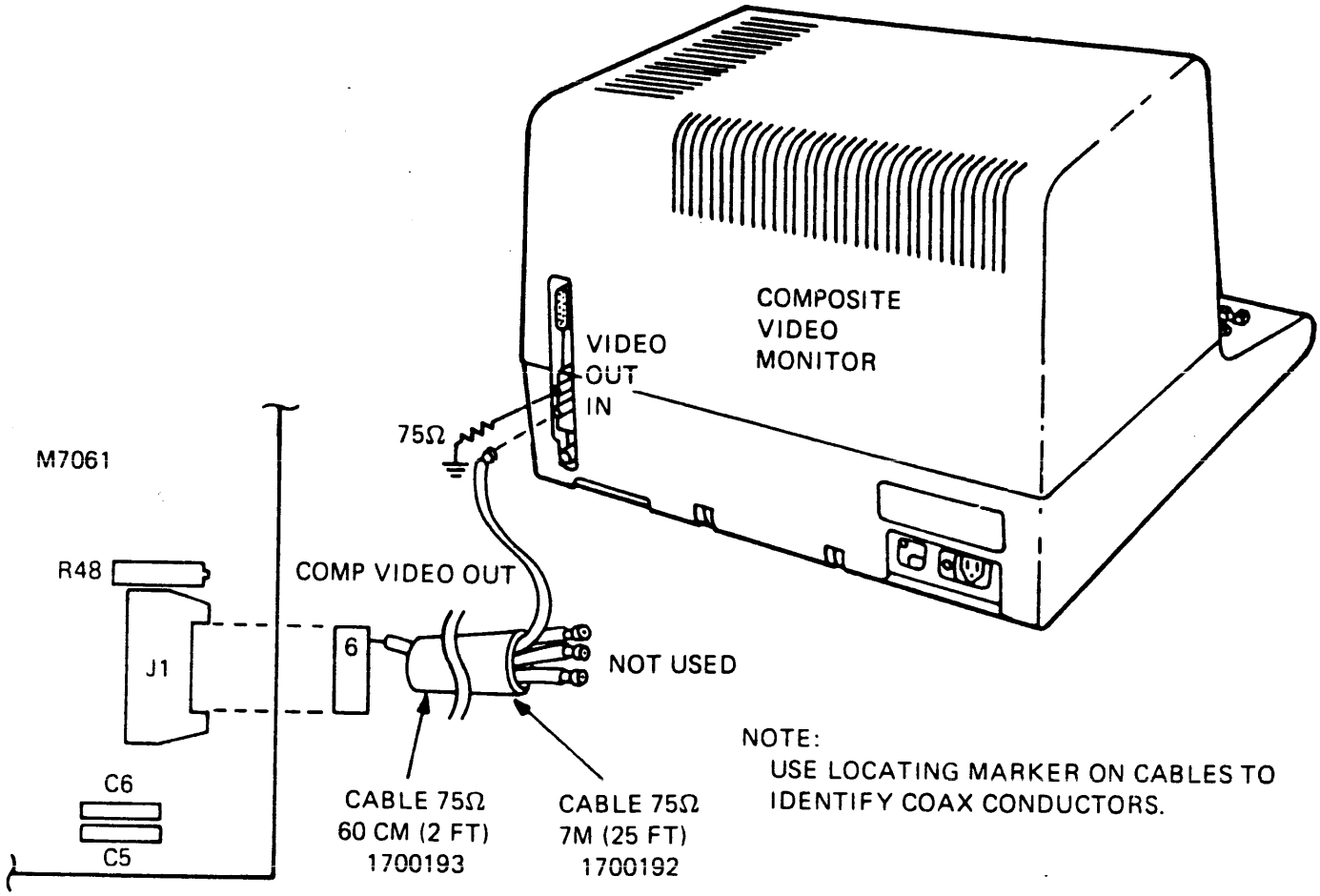


Figure 2-22
Monochrome Composite Video Monitor Installation

E.2 Connection of VT100-LA/LB -- referring to Figure 2-23, execute the following steps, then proceed to Step F.

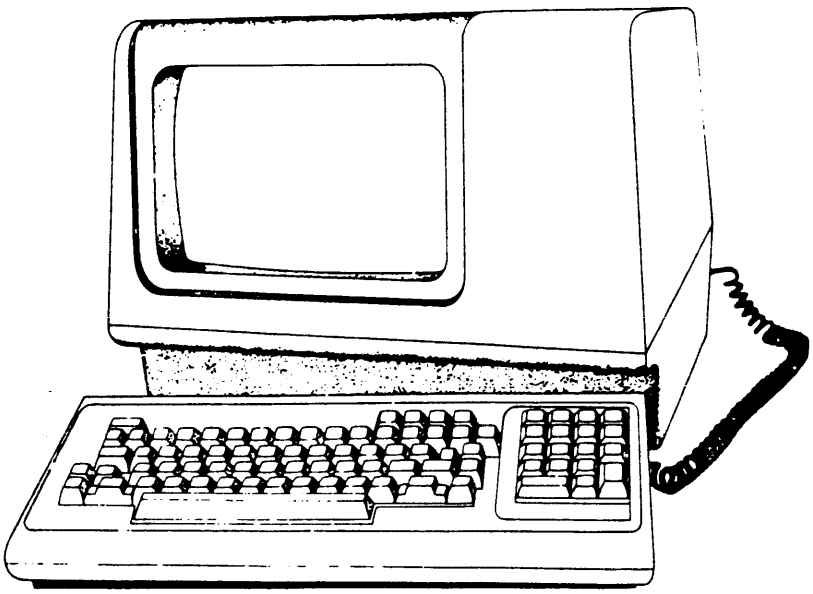
1. Identify the 2-foot 5-Conductor coaxial pigtail cable with BNC connectors on one end and an AMP connector on the other (P/N 17-00193), and the long 4-conductor coaxial Monitor cable with BNC connectors on both ends.

2. Identify the conductor marked with the black locating marker (band) on each cable; this is conductor #1, with corresponding BNC connectors J1 and P1. Refer to drawing D-UA-VSV11-0-0 and drawing C-IC-VSV11-0-4, sheet 1, and connect J1 on the pigtail cable to P1 on the Monitor cable. Similarly, connect J2 to P2 (the connectors adjacent to J1 and P1 when the cable is laid flat).

3. Connect the "J1" BNC connector on the Monitor cable to the "VIDEO IN" connector on the VT100-LA/LB. Similarly, connect the "J2" BNC connector to the "VIDEO OUT" connector on the VT100-LA/LB.

4. Observe the Key and/or "G" and "S" markings on the AMP connector on the pigtail cable. Insert the AMP connector into header J1 on the M7061 Sync Generator module, with the "G" marking nearest the the module.

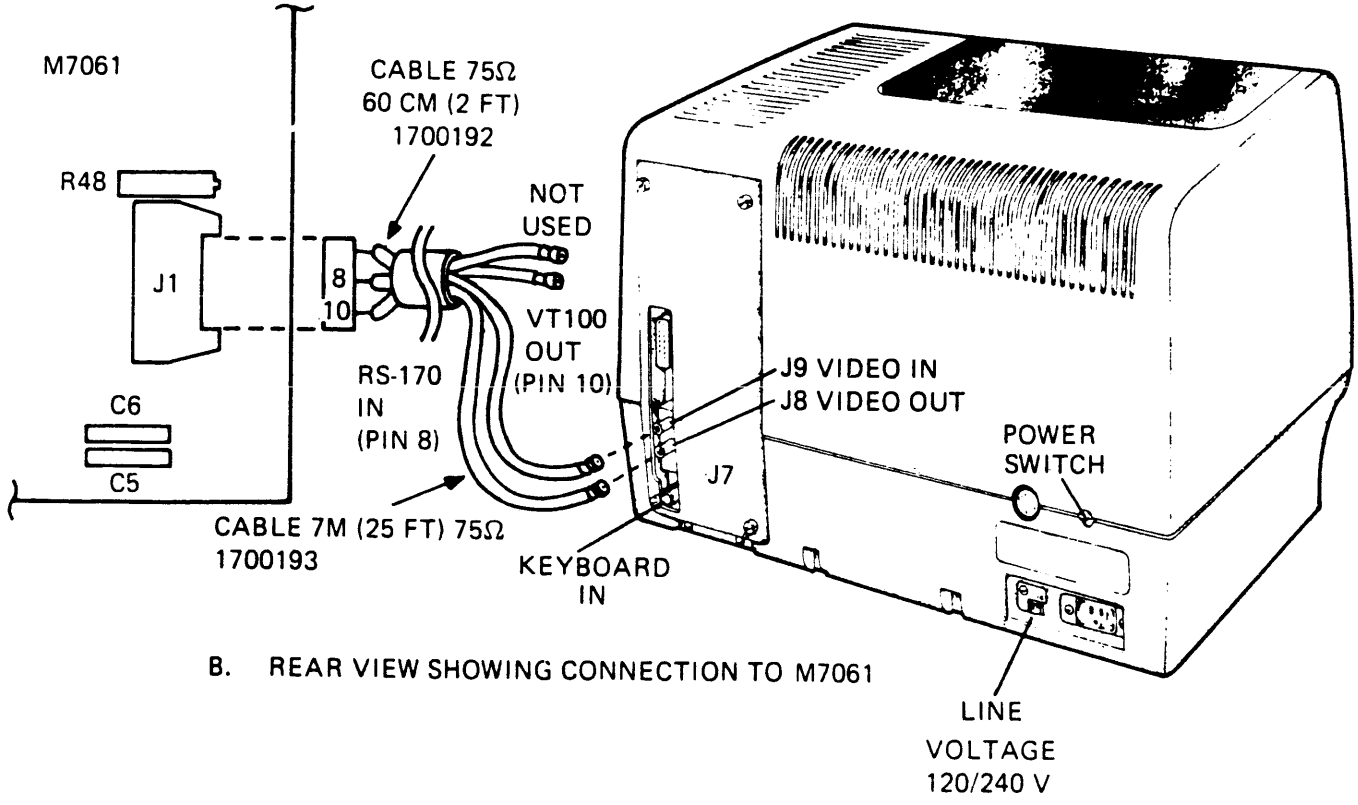
5. Proceed to Step F.



A. FRONT VIEW SHOWING KEYBOARD PLACEMENT

NOTE

USE LOCATING MARKER ON CABLES TO IDENTIFY COAX CONDUCTORS.



B. REAR VIEW SHOWING CONNECTION TO M7061

MR-1828

Figure 2-23
VT100-LA/LB Monochrome Monitor Installation

E.3 Connection of VRV02-BA/BB -- referring to Figure 2-24, execute the following steps, then proceed to step F.

1. Identify the 2-foot 5-Conductor coaxial pigtail cable with BNC connectors on one end and an AMP connector on the other (P/N 17-00193), and the long 4-conductor coaxial Monitor cable with BNC connectors on both ends.

2. Identify the conductor marked with the black locating marker (band) on each cable; this is conductor #1, with corresponding BNC connectors J1 and P1. When the cables are laid flat the conductors and BNC connectors are numbered in order from #1 (the conductor with the black band). Refer to drawing D-UA-VSV11-0-0.

3. Refer to drawing C-IC-VSV11-0-4, sheet 2, and connect J3 on the pigtail cable to P1 on the Monitor cable. Connect the other end of this conductor (with the black band) to one of the GREEN inputs on the rear of the CRT monitor cabinet.

4. Connect J4 and J5 of the pigtail cable to P2 and P3, respectively, of the Monitor cable. Then connect J2 and J3 at the other end of the Monitor cable to the BLUE, and RED inputs, respectively, at the rear of the CRT monitor cabinet.

5. Connect J2 on the pigtail cable to P4 on the Monitor cable; then connect the other end of this conductor to the "VIDEO OUT" connector on the VRV02 Keyboard Interface box.

6. Observe the Key and/or "G" and "S" markings on the AMP connector on the pigtail cable. Insert the AMP connector into header J1 on the M7061 Sync Generator module, with the "G" marking nearest the the module.

7. Proceed to Step F.

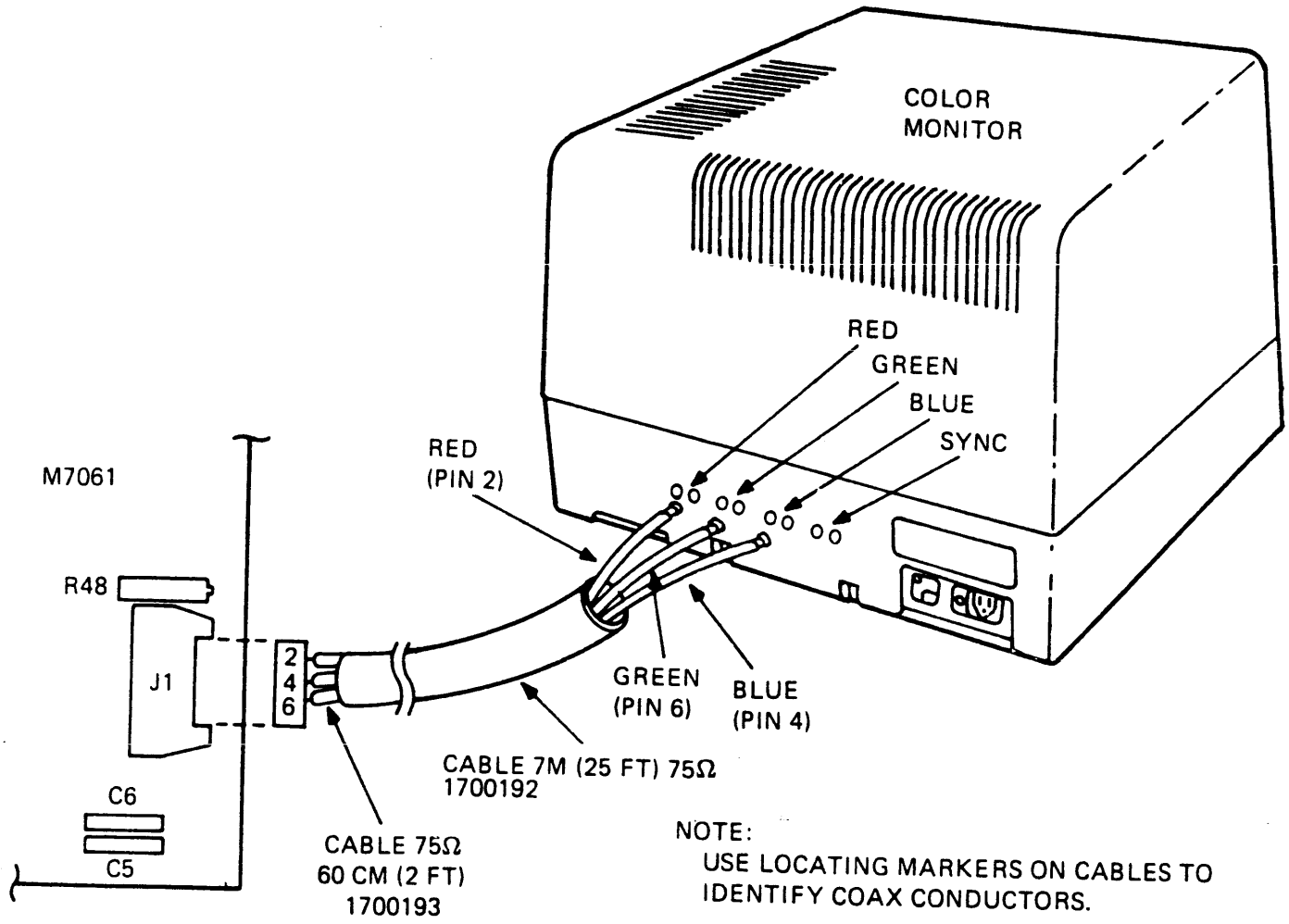


Figure 2-24
VRV02-BA/BB Color Monitor Installation

F. Joystick (H3060) Connection

The H3060 Joystick is connected to the VSV11/VS11 system at 10-pin connector J3 on the M7061 module, via a Joystick pigtail cable and a long cable attached to the Joystick itself. The pigtail cable has a Berg-type connector on the module end and a Cinch connector on the end connecting to the Joystick cable. Figure 2-25 illustrates the J3 connector pinning, and Figure 2-26 illustrates the H3060 Joystick and its cable.

Refer to drawings C-IC-VSV11-04 and D-UA-VSV11-0-0 and connect the Joystick pigtail cable (P/N 70-15822) to J3 of the M7061 Sync Generator module (with the label "UP" facing out from the module). Then connect and secure the Cinch connectors on the pigtail and the cable attached to the H3060 Joystick assembly. Then proceed to Step G.

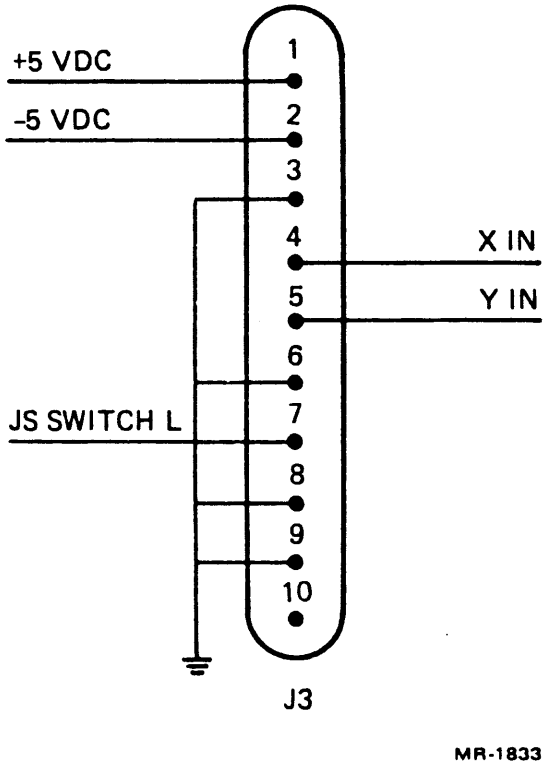


Figure 2-25
Joystick Connector Pin Assignments

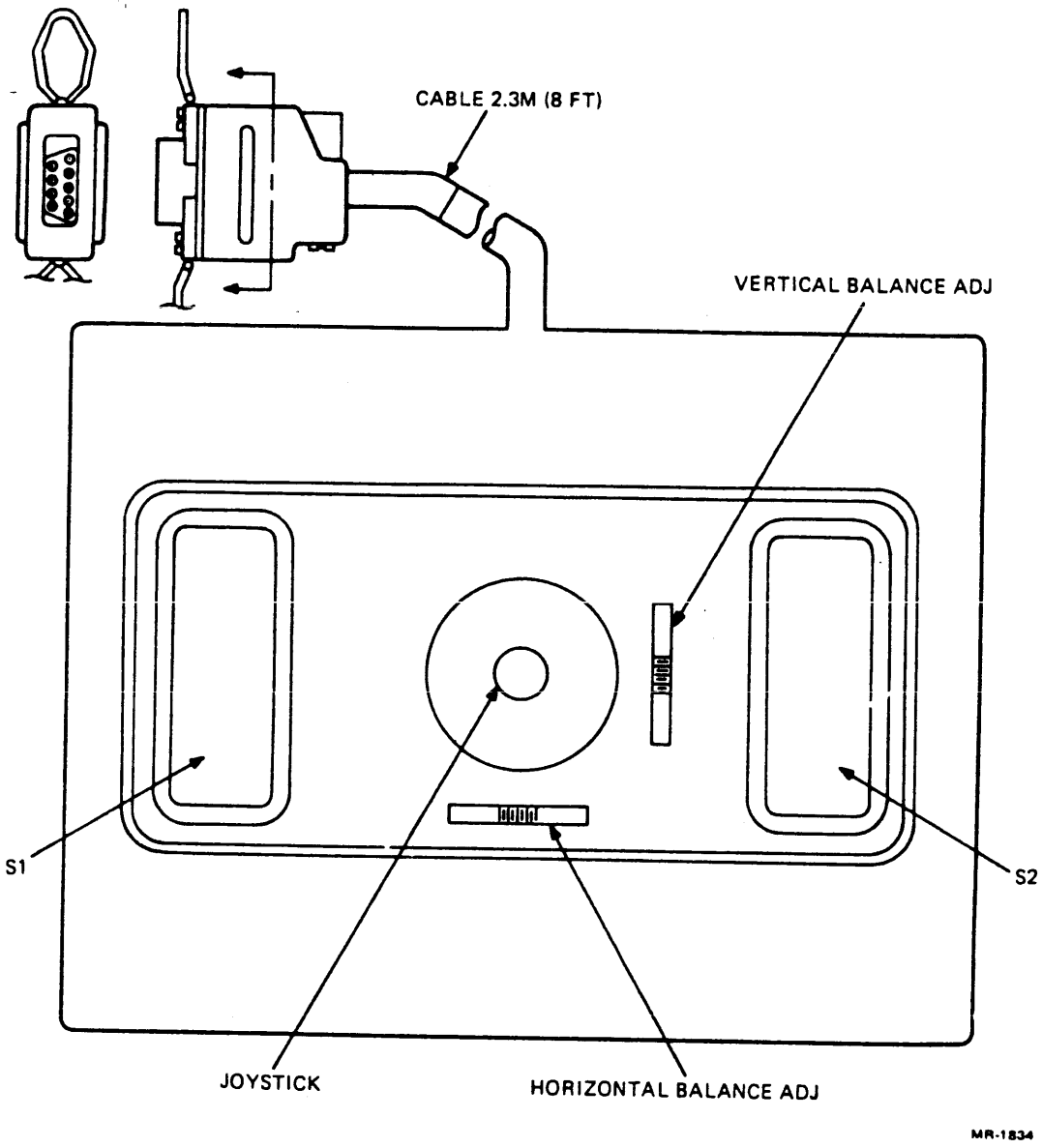


Figure 2-26
H3060 Joystick Assembly

G. If the monitor was supplied with the VSV11/VS11, connect the serial communication cable between the COMM connector on the monitor and the host computer.

2.5 CHECKOUT

Make sure system and monitor power is ON and load the VSV11/VS11 test program [CVVSA for PDP-11 and LSI-11 systems; EVTCB (Level 3 Diagnostic) for VAX systems] and perform the following checkout procedure. If trouble arises, or if adjustments need to be made (e.g., to the M7061 Sync Generator or the monitor), refer to Chapter 7, Tables 7-1 and 7-2, for troubleshooting and adjustment procedures.

A. Initial Checks and Adjustments

If the system being installed is a VSV11/VS11-AA, -AB, -AC, or -AD, there are no initial adjustments required (since sync is generated internally by a crystal oscillator); therefore, proceed directly to Step B and begin checkout using the diagnostic program.

If the system is supplied with a monitor, the External Sync mode of operation is being used and initial adjustments may be required. Proceed as follows:

1. Refer to Figure 2-7 and locate on the M7061 module potentiometer R48, the control for adjusting the input gain for the external sync signal (supplied from the VRV02 Keyboard Interface box or from the VT100). Set this potentiometer to the middle of its range, 12.5 turns from either end of its travel.

2. If the system is a VSV11/VS11-AE, -AF, -AH or -AJ (supplied with VT100-LA/LB monochrome monitor), proceed to Step B, since further adjustment requires the services of the diagnostic program. If a color monitor (VRV02-BA/BB) is being used, proceed to the next step below.

3. With power on but the CPU initialized, turn up the brightness contrast controls (fully clockwise) on the front of the display monitor.

4. Observe the screen. A raster (many fine parallel horizontal lines) should be observed. In addition, a "sync tab" (short blanked block at the center of the lower edge of the screen) should be observed. Press the SET-UP key on the VRV02 keyboard; the standard set-up frame should be visible. If no raster or set-up frame is visible, refer to Table 7-2, the Video and VRV02 troubleshooting chart, in Chapter 7 and recheck the cabling, monitor power, etc.

5. Perform the adjustment procedure given in Paragraph 7.5 to properly adjust potentiometers R48 and R9 on the M7061 module. This procedure requires the use of an oscilloscope and it is highly recommended that the

procedure be followed for proper setup. If an oscilloscope is not available, adjust potentiometer R9 until the image is stable. If the image cannot be stabilized by adjusting only R9, also adjust R48 but do not turn it too far clockwise as this will decrease the input gain and lead to unstable timing. If the image cannot be stablized, refer to the troubleshooting procedures in Table 7-2. When the raster and set-up frame are stable, proceed to Step B.

B. Basic Logic Checkout

Run the basic (default) series of tests for the unit. Follow the loading and operating procedures supplied in the program listing. The program should run two passes of Tests 1 through 32 without error. The examples given below show the typical sequence of operations used for running the programs. In the examples, typed entries to be supplied by the operator are underlined; prompts and other output from the Diagnostic Supervisor are not underlined and should not be typed. Enter a Carriage Return when the <cr> symbol is given. After two passes of the test sequence have been run, proceed to Step C.

For PDP-11 or LSI-11 systems, the following procedure should be used:

1. Boot the diagnostic medium and answer any questions presented.

2. Load and initiate the VSV11/VS11 test program by typing:

   .R CVVSA<cr>

3. When the program is loaded and initiated, it will identify itself and respond with the "DR>" prompt.

4. To start the basic section of tests, respond to the prompt by typing:

   DR> STA/FLA:HOE:PNT<cr>

5. The supervisor will respond with questions asking for the VS11 hardware parameters: number of units (answer "1"), device (DPC) address, interrupt vector address, BR level, whether a Lookup Table (LUT) is installed, and whether the unit is running in 50Hz mode. Answer these appropriately, either by typing in a new entry followed by a carriage return, or by just typing a carriage return to keep the entry already present. A typical sequence would be:

```
CHANGE HW (L) ? Y<cr>

# UNITS (D) ? 1<cr>

UNIT 0
DEVICE ADDRESS          (O) 172010 ? 172000<cr>  (Select 172000)
1ST INTERRUPT VECTOR    (O) 320 ? <cr>           (Keep 320)
INTERRUPT PRIORITY      (O) 4 ? 6<cr>            (Change to BR6)
LUT INSTALLED           (L) N ? <cr>             (Not Available)
FREQUENCY = 50HZ        (L) N ? <cr>             (Keep 60Hz)
```

The program will then ask if software operating parameters are to be changed; answer NO by typing N<cr>.

6. The tests will run in sequence, with the number and name of each test printed as it is executed. If an error is encountered, control will return to the diagnostic supervisor after the error report is printed.

7. If it is desired to stop the test sequence at any time, type Control-C (hold the CTRL key down and type C); control will return to the Diagnostic Supervisor. In order to restart the program without changing the hardware parameters, type:

   DR> RES/FLA:HOE:PNT

For VAX systems, the following procedure should be used:

1. Boot the diagnostic medium containing the Diagnostic Supervisor and the VS11 Level 3 Diagnostic, EVTCB.

2. The Diagnostic Supervisor will load and initiate itself. It will issue an identification message and the "DS>" prompt.

3. Following the prompt, load the VS11 Diagnostic by typing:

   DS> LOAD EVTCB<cr>

4. When the program is loaded, the supervisor will again respond with the "DS>" prompt.

5. Proceed to set up the operating environment by ATTACHing the UNIBUS Adapter (DW780) and the VS11 to the supervisor by typing the following (the DS> prompts are shown for clarity but should not be typed):

   ```
   DS> ATTACH DW780 SBI DWO 3 4<cr>
   DS> ATTACH VS11 DWO VSO 767010 720 6 N N N<cr>
   DS>
   ```

Note that the parameters given in the ATTach strings are an example; the actual parameters entered may be different. Also, if it is desired that the "long" form of the Attach commands be used, in which each parameter is listed in sequence with a wait for a specific reply, merely type ATT<cr> and answer each question.

6. Select the VS11 for testing by typing:

   DS> SELECT VS0<cr>

7. It is recommended that the program be run in "Trace" mode (allowing the name of each test in the program to be printed as it is initiated) with "Halt on Error" enabled. Do this by typing:

   DS> SET FLAG TRACE,HALT<cr>

8. Start the test sequence by typing:

   DS> START/PASS:2<cr>

C. Configuration Checkout

Run TEST 35, the "Configuration Typeout" test in the Standalone section of the Diagnostic Program.

For the PDP-11, start the test by typing:

DR> RES/TES:35<cr>

For the VAX, start the test by typing:

DS> ST/TE:35/SEC:STANDALONE

Observe the resultant printout. Each Image Memory channel and Sync Generator channel detected by the program is listed, along with various parameters. For this test, there should be one Memory channel (channel 0), with 4 bits of data, with a "MEMTAB" value of 001700. There should also be one Sync channel (channel 0). The "SYCTAB" value and the "NON-INTERLACED" or "INTERLACED" message depend upon the specific model of VSV11/VS11 at hand. For systems with one M7062 Image Memory, verify that the SYCTAB value is 100000 and "NON-INTERLACED". For systems with two M7062 Image Memories, the SYCTAB value should be 120000 and "INTERLACED"

The correct printout for systems with one M7062 Image Memory module is:

```
MEMORY:     0,  MEMTAB VAL:  001700,  4 BITS
SYNC CHAN:  0,  SYCTAB VAL:  100000,  NON-INTERLACED
```

The correct printout for systems with two M7062 Image Memory modules is:

```
MEMORY:     0,  MEMTAB VAL:  001700,  4 BITS
SYNC CHAN:  0,  SYCTAB VAL:  120000,  INTERLACED
```

Return to the diagnostic supervisor by typing Control-C.

D. Video Checkout

In order to checkout and verify the operation of the generation, transmission, and display of video data, perform the following steps:

1. Run TEST 34, "SELECTED DISPLAYS", in the Diagnostic.

   For the PDP-11, start the test by typing:

   DR> RES/TES:34<cr>

   For the VAX, start the test by typing:

   DS> ST/TE:34/SEC:STANDALONE

2. Observe the "menu" of available displays and select each one in order, beginning at item #3. Observe the display monitor carefully after each selection. If a display is not seen, adjust the brightness and/or contrast on the monitor. Many of the displays have a perimeter outline, which should be about 9.5 inches square and should be centered on the screen. If the display is not as expected, or lacks quality, refer to the troubleshooting procedures in Chapter 7.

3. For each selection (except 0, 1 and 2), the display should be stable and present the picture described in the menu.

4. For color monitors, select item 7 and verify that the proper colors correspond to the labels.

5. Verify the BLINK feature by alternately selecting items 1 (BLINK ON) and 2 (BLINK OFF) while displaying each of the pictures in items 3 through 8. When BLINK is ON, any White line or area (on a color monitor) should blink on and off 4 times per second. Specifically, in any display with a perimeter outline of the screen, the outline should blink. Further, in display #8, any color (shade on Monochrome systems) with LSB GRN (Least- significant GREEN bit) set should blink.

6. If the monitor is a VT100-LA/LB or VRV02-BA/BB, select item #5 (Crosshatch) and press the SET-UP key on the keyboard to display the familiar set-up frame. The video intensity of the crosshatch should be equal to the intensity of the characters in the set-up frame. If the intensities are not equal, refer to Paragraph 7.5 and Table 7-2 (Chapter 7) and adjust potentiometers R48 and R9 on the M7061 module.

7. If R48 and/or R9 had to be adjusted in the previous step, repeat steps 2, 3 and 4 and observe the picture quality. If the quality is not acceptable, further adjustments to the monitor and/or M7061 may be required. Refer to Table 7-2.

8. Select Item #9 of Test 34 (solid white square) to check a VRV02 monitor's color balance. There are two color balances which must be properly adjusted to obtain a white display over a range of contrast control settings. The first consists of the Brightness white balance, and the second is Contrast white balance. White balance is determined by displaying the white square and then observing the square for color changes while adjusting the front-panel Contrast control over its lower range. You can expect the display to bleed or become fuzzy at high settings of this control. If not appreciable variation of the white square is observed, both adjustments are properly balanced. If the display color does vary, refer to the white balance adjustment procedures in Table 7-2.

9. Type Control-C to return to the Diagnostic Supervisor and proceed to the next step.

E. Joystick Checkout

In order to check out the Joystick and associated logic, run TEST 33 and perform the following steps:

1. Start the test by typing:

   DR> RES/TES:33<cr> (for PDP-11)

   or

   DS> ST/TE:33/SEC:ST (for VAX)

2. Observe that the cursor (a small white "cross") is placed near the lower left-hand corner of the screen and that it is indeed small and white.

3. In the upper right-hand corner of the screen are displayed the cursor X-Y coordinates. Verify that both JSX and JSY read 0100.

4. The screen should contain a set of concentric boxes with position labels along the sides.

5. Operate the Joystick lever; the cursor should move in response to the direction of lever position and the displayed coordinates should change accordingly.

6. Verify the Joystick SWITCH interrupt by moving the cursor to a blank area of the screen and pressing one of the rectangular switches on the Joystick assembly on either side of the lever. When the switch is pressed, a small "X" should appear at the cursor position.

7. Move the cursor, press the switch again and verify that the "X" now appears at the new cursor position.

8. Move the cursor onto one of the lines of one of the boxes and press the Joystick switch. The "X" should appear at that position and the word "MATCH" should appear below the display coordinates at the upper right. One of the coordinates should correspond to the label on the line where the cursor is positioned.

9. Verify that a MATCH occurs when the cursor is moved into the solid white box in the center of the screen and the switch is pressed.

10. Verify that the cursor does not drift when the Joystick lever is in its center (rest) position. If drift occurs, the trimming potentiometers on the Joystick assembly should be adjusted.

11. Exit the Joystick test by typing Control-C and proceed to the next step.

F. Terminal Test

If the monitor was supplied with the VSV11/VS11 system, it should function as a normal computer terminal. Verify that this is so by running the appropriate terminal diagnostic on the host computer or, alternatively, just logging in and performing some useful functions.

G. System Test

For PDP-11 and LSI-11 systems, the VSV11/VS11 is supplied with a DEC-X/ii System Exerciser module. Configure a DEC-X/11 System Exerciser including all devices in the system and run it until a complete "relocation cycle" through memory is made.

For VAX-11 systems, the VS11 Level 2 diagnostic, EVTCA, is supplied. This program runs under VMS and is similar to the Level 3 diagnostic used above. EVTCA contains 16 tests in the Default section corresponding to some of the tests in the Default section of EVTCB. It also contains a Joystick Verification test and a Selected Displays test. Operation is almost identical to that for the Level 3 program, except that the ATTACH statement does not contain specifications for DPU-Only mode, Long Memory Tests, or Frequency. Run the Default section for 2 passes. Then perform Video Checkout and Joystick Checkout as in Steps D and E above, respectively.

2.6 CUSTOMER CONFIGURATION

The procedures presented in the preceeding paragraphs will leave the VSV11/VS11 system set up in the optimum general-purpose configuration. It is recommended that it be left this way. The customer may elect, however, to make use of the optional functionality built into the VSV11/VS11, such as:

1. Cursor Size: Large full-screen cursor versus the standard small cursor,

2. Cursor Color: Green, Green + Blue, or Green + Red, versus the standard White,

3. Blink Rate: Can be slowed to 2 times per second, once every second, or once every 2 seconds, versus the standard 4 times per second,

4. Video Output DAC Control: 8 Shades/Colors, whereby the least- significant Green bit [Blink Data] is ignored, versus the standard 16 Shades/Colors,

5. Dual Non-Interlaced Image Memory Channels (each with 512 x 256 4-bit pixels) versus one Interlaced channel (with 512 x 512 4-bit pixels) for "dynamics" on systems with two M7062 Image Memory modules,

6. Interlaced Operation versus the standard Non-Interlaced mode, for systems with a single M7062 Image Memory for finer spacial resolution (512 x 512 pixels) at the expense of pixel intensity resolution (2 bits per pixel). This change would most likely be useful only in a Monochrome (Black & White) system.

If no changes are to be made, proceed directly to Paragraph 2.7 to perform acceptance on the system.

The following paragraphs discuss the changes that can be made. If the customer does elect any of the options, the conversions should be performed at this time, by changing switch and jumper settings on the M7061 and M7062 modules using the procedures described in the following paragraphs. After all changes have been made, record the final switch and jumper settings for future reference. Then perform checkout of the VSV11/VS11 system as described in Paragraph 2.6.4.

2.6.1 Available Configuration Changes

Table 2-13 lists the functions available on the M7061 Sync Generator module, the corresponding switch and jumper settings, and how they were set to the standard configurations in the previous procedures. If changes are being made, remove power from the system, remove the M7061 module and make the desired

changes; refer to Table 2-13, Figure 2-7, and the following list. If the Image Memory configuration is being changed, also refer to Paragraph 2.6.2 or 2.6.3. Take care not to disturb the switch and jumper settings of functions not being changed.

There are four types of functions selected by the switches and jumpers listed in Table 2-13:

1. Fixed Functions, which should not be changed from the settings given. These are:

   (a) RS170-In Gain
   (b) Special Scan
   (c) Master/Slave
   (d) Channel Number

2. Model-Independent Functions, which can be selected according to customer preference using the settings given in Table 2-13 without changing the basic functioning of the system. These are:

   (a) Cursor Color
   (b) Cursor Size
   (c) Blink Rate
   (d) Video Output DAC Control

3. Monitor-Dependent Functions, which can be changed if the monitor is supplied with the VSV11/VS11 (i.e., if the monitor is a VT100-LA/LB or VRV02-BA/BB) or if the customer-supplied monitor is compatible with the desired changes. These are:

   (a) Operating Frequency (Field Rate): Can be changed from 60 Hz to 50 Hz or vice-versa by changing switches E21-1 and E21-2 and changing the frequency of the monitor by using the SET-UP operation (see Appendix C). This change would most likely be used on a 60 Hz system if 256 (Non-Interlaced) or 512 (Interlaced) visible scan lines are desired, as opposed to the normal 240 or 480 visible scan lines. In a 50 Hz system, flicker can be reduced in the Interlaced mode by running the monitor at 60 Hz, but the number of visible scan lines is reduced from 512 to 480.

   (b) SYNC Timing Base: The normal External mode used with the supplied VRV02-BA/BB Color Monitor can be changed to Internal mode if it is not desired that the Keyboard output appear on the monitor.

4. Image Memory-Dependent Functions:

   (a) For systems with one M7062 Image Memory

module, normally set up for Non-Interlaced operation resulting in 240 (or 256) visible scan lines with each pixel containing 4 bits, the Memory (M7062) and Sync (M7061) modules can be set up for Interlaced operation. Paragraph 2.6.2 describes the set-up procedure in detail.

(b) For systems with two M7062 Image Memory modules, normally set up as a single channel in Interlaced mode with 480 (or 512) visible scan lines with each pixel containing 4 bits, the Sync Generator (M7061) module and both Memory (M7062) modules can be set up for Non-Interlaced operation, with one memory remaining at Channel #0 and the other changed to Channel #1. Alternatively, both channels can be set up for Interlaced operation, with each channel containing 512x512 2-bit pixels. Paragraph 2.6.3 describes the set-up procedure in detail.

Table 2-13
M7061 Sync Generator Switch/Jumper Functions

FUNCTION	SWITCHES/JUMPERS	SELECTIONS	VSV/VS11 Models at Initial Settings
Operating Frequency (Field Rate)	E21-1 E21-2 OFF ON ON OFF	60 Hz - - - - - - + 50 Hz - - - - - - +	-AA, AC, AE, AH, AP, AS -AB, AD, AF, AJ, AR, AT
Scan Mode/ Resolution	E21-3 E21-9 ON ON OFF ON OFF OFF	Non-Interlaced - + Interlaced - + Special	-AA, AB, AE, AF, AP, AR -AC, AD, AH, AJ, AS, AT
Special Scan	E21-4 E21-5 OFF ON ON OFF	Normal - - - - - + Special	All Models
Master/ Slave	E21-6 W19 ON IN OFF OUT	Master - - - - - + Slave	All Models
SYNC Timing Base	E21 E21 E21 -7 -8 -10 W3 OFF ON ON OUT ON OFF OFF IN	Internal (XTAL) + External (RS170) +	-AA, AB, AC, AD -AE thru -AT
RS170-In Gain	W4 IN OUT	Adjustable - - - + Fixed	All Models
Channel Number	W5 W6 W7 W8 OUT IN OUT IN OUT IN IN OUT IN OUT OUT IN IN OUT IN OUT	Channel #0 - - - + Channel #1 Channel #2 Channel #3	All Models
Cursor Color	W10 W11 IN IN IN OUT OUT IN OUT OUT	White - - - - - + Green + Blue Green + Red Green	All Models
Blink Rate	W12 W13 W14 IN IN IN OUT IN IN IN IN OUT OUT OUT IN	4 Times per Sec. + 2 Times per Sec. 1 Time per Sec. Once per 2 Sec.	All Models
Cursor Size	W16 W17 IN IN OUT OUT	Small (16x16) - + Large (Full)	All Models
Video Output DAC Control	W21 W22 OUT IN IN OUT	16 Shades/Colors + 8 Shades/Colors	All Models

2.6.2 Non-Interlaced To Interlaced Conversion

The standard setup for systems with one Image Memory (M7062) module results in a single memory channel (Channel 0) supplying 4 bits of pixel data. Operation is Non-Interlaced, resulting in a display with a resolution of 512 horizontal pixels and 240 (60 Hz) or 256 (50 Hz) vertical pixels. (The viewing area is still 480 (or 512, 50Hz) high, but only alternate lines are displayed.) The M7062 switch settings for this configuration are given in Table 2-3. On the M7061, switches E21-3 and E21-9 are configured to the Non-Interlaced mode. Figure 2-1 depicts the standard single-memory configuration, in which the M7062 is set up to handle four data bits per pixel. The data is supplied from Data Bus (DBUS) bits <9:6> and driven onto Video Bus bits <7:4>.

The optional Interlaced memory configuration is shown in Figure 2-27. In order to change the system to this mode, turn switch E21-3 OFF on the M7061 Sync Generator module. Then configure the switches on the M7062 Image Memory module according to Table 2-14. Finally, using the SET-UP procedure for the VT100-LA/LB or VRV02-BA/BB, change the operating mode of the monitor to Interlaced (i.e., toggle the last digit in option group 3 in the SETUP-B frame from 0 to 1) and store the new set-up information by typing SHIFT/S.

After the changes are complete, proceed to Paragraph 2.6.4 to check out the new configuration using the diagnostic program. When running Test 35, the System Configuration Type-out test, the resulting printout should be:

```
MEMORY:     0,   MEMTAB VAL:  001400,   2 BITS
SYNC CHAN:  0,   SYCTAB VAL:  120000,   INTERLACED
```

When running Test 34, Selected Displays, select menu item 8. Observe the display and verify that only four distinct shades exist, corresponding to the four combinations of MSB-GRN (DBUS 9) and LSB-GRN (DBUS 8).

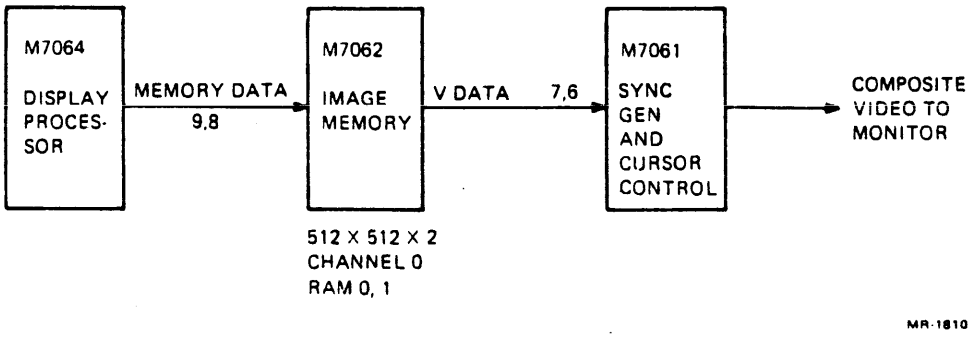


Figure 2-27
Single Interlaced Image Memory Block Diagram

Table 2-14
M7062 Switch & Jumper Setup (2-Bit Interlaced Memory)

Switch No.	E59	E49	Effect
1 2	ON ON	ON ON	Set pixel data width to 2 bits by internally connecting the least-significant RAM bits (1,0) to the most-significant RAM bits (3,2).
3 4	ON ON	ON ON	Connect DBUS <9:8> to the input of the 2-bit RAM; connect output of the 2-bit RAM to VBUS <7:6>. These bits are, respectively, the most-significant DBUS and VBUS data bits.
5 6 7 8 9 10	OFF OFF OFF OFF OFF OFF	OFF OFF OFF OFF OFF OFF	The least- significant 6 bits of the DBUS and VBUS are not connected to the Image Memory.

Function	Jumper(s)				Selection
DATA AVAILABLE Enable	W1 IN				Enabled. Always leave installed.
M-SYNC Enable	W2 IN				Enabled. Always leave installed.
Channel Number	W3	W4	W5	W6	
	OUT	OUT	IN	IN	Channel #0
	OUT	IN	IN	OUT	Channel #1
	IN	OUT	OUT	IN	Channel #2
	IN	IN	OUT	OUT	Channel #3
					On multi-channel systems, assign channels in order, starting at 0.

2.6.3 Conversion To Dual-Memory System

The standard setup for systems with two Image Memory (M7062) modules, shown in Figure 2-2, results in a single memory channel (Channel 0) supplying 4 bits of pixel data. Operation is Interlaced, resulting in a display with a resolution of 512 horizontal pixels and 480 (60 Hz) or 512 (50 Hz) vertical pixels. The M7062 switch settings for this configuration are given in Table 2-4. On the M7061, switches E21-3 and E21-9 are configured to the Interlaced mode. Figure 2-2 depicts the standard single-channel configuration, in which each M7062 is set up to handle two data bits per pixel. For module 1, the data is supplied from Data Bus (DBUS) bits <9:8> and driven onto Video Bus (VBUS) bits <7:6>; these are the two Green bits. For module 2, the data is supplied from DBUS bits <7:6> and driven onto VBUS bits <5:4>; these are the Red and Blue bits.

The optional 2-channel Non-Interlaced memory configuration is shown in Figure 2-28. In order to change the system to this mode, turn switch E21-3 ON on the M7061 Sync Generator module. Then configure the switches on both M7062 Image Memory modules according to Table 2-15. On Module 2 (the module without resistor packs installed in E76 and E77) install jumper W4 and remove jumper W6 in order to change it from Channel 0 to Channel 1. When reinstalling the modules in the backplane, place M7062 #1 (with resistor packs installed in E76 and E77) nearest the M7061 Sync Generator. Finally, using the SET-UP procedure for the VT100-LA/LB or VRV02-BA/BB, change the operating mode of the monitor to Non-Interlaced (i.e., toggle the last digit in option group 3 in the SETUP-B frame from 1 to 0) and store the new set-up information by typing SHIFT/S.

After the changes are complete, proceed to Paragraph 2.6.4 to check out the new configuration using the diagnostic program. When running Test 35, the System Configuration Type-out test, the resulting printout should be:

```
MEMORY:     0,  MEMTAB VAL: 001700,  4 BITS
MEMORY:     1,  MEMTAB VAL: 001700,  4 BITS
SYNC CHAN:  0,  SYCTAB VAL: 100000,  NON-INTERLACED
```

As a final check, run Test 34, Selected Displays, and select menu item 8. Observe the display and verify that 16 distinct shades exist.

[Note that the two memory channels could also be configured for Interlaced operation, with each channel set up for 512x512x2 bits. If this is the case, configure the switches and jumpers on both M7062 modules according to Table 2-14, with one module set up for Channel 0 and the other for Channel 1. Then turn switch E21-3 OFF on the M7061 module.]

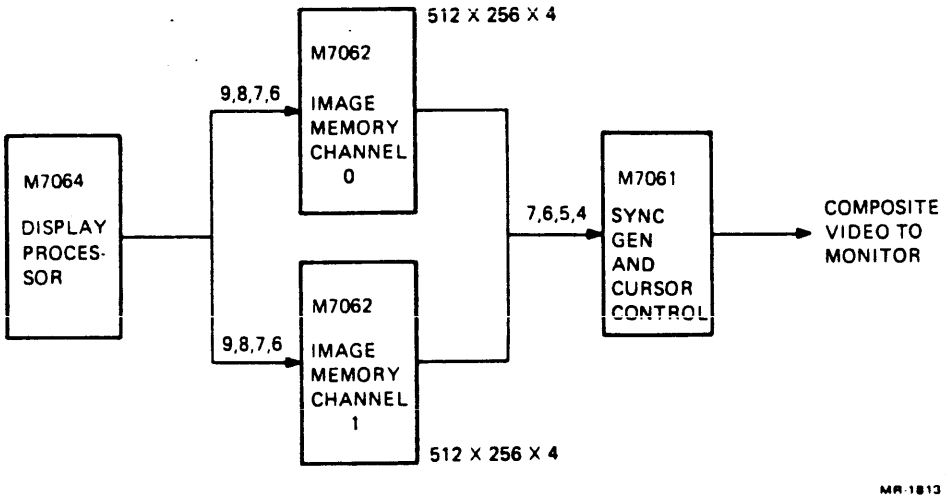


Figure 2-28
Dual-Channel Non-Interlaced Image Memory Block Diagram

Table 2-15
M7062 Switch & Jumper Setup (4-Bit Non-Interlaced)

Switch No.	E59	E49	Effect
1 2	OFF OFF	OFF OFF	Set pixel data width to 4 bits.
3 4 5 6	ON ON ON ON	ON ON ON ON	Connect DBUS <9:6> to the input of the 4-bit RAM; connect output of the 4-bit RAM to VBUS <7:4>. These bits are, respectively, the four most- significant DBUS and VBUS data bits. They are defined as follows: DBUS VBUS Definition 9 7 MSB-Green 8 6 LSB-Green 7 5 Red 6 4 Blue
7 8 9 10	OFF OFF OFF OFF	OFF OFF OFF OFF	The least- significant 4 bits of the DBUS and VBUS are not connected to the Image Memory.

Function	Jumper(s)	Selection
DATA AVAILABLE Enable	W1 IN	Enabled. Always leave installed.
M-SYNC Enable	W2 IN	Enabled. Always leave installed.
Channel Number	W3 W4 W5 W6 OUT OUT IN IN OUT IN IN OUT IN OUT OUT IN IN IN OUT OUT	Channel #0 Channel #1 Channel #2 Channel #3 On multi-channel systems, always assign channels in order, starting at 0.

2.6.4 Checkout Of Changes

After all switch and jumper changes have been made and verified, reinstall any modules or cables removed. Then run two passes of the normal (default) test series of the diagnostic (Tests 1 through 32). No errors should be encountered. Reflect any change in operating frequency (50/60 Hz) in the startup dialog for the program.

Run Test 35, System Configuration Typeout, and verify that the system configuration is as expected.

Run Test 33, Joystick Verification, and verify that the cursor size and color are as expected.

Run Test 34, Selected Displays, and verify that:

1. The perimeter outline, Selection 6, reaches the top of the screen.

2. The expected shades/colors are present (Selection 8),

3. The blink rate is as expected.

When all checks are complete, proceed to Paragraph 2.7 to perform Acceptance.

2.7 ACCEPTANCE

Neatly arrange all cables and return mounting boxes to their normal positions with covers secured.

Perform Option Acceptance by repeating the diagnostic test procedures given in Paragraph 2.5.

2.8 EXTENDED CONFIGURATIONS

The previous paragraphs describe the installation of VSV11 and VS11 systems containing only one M7061 Sync Generator module and either one or two M7062 Image Memory modules. These are the VSV11/VS11-Ax series of model designations. For VS11 systems, these are the maximum configurations that will fit within the standard DDV11-CK 4-slot backplane supplied with the DW11-BK.

If necessary, the basic configurations can be expanded by the addition of M7061 Sync Generator modules (to drive independent monitors) and/or M7062 Image Memories (to support additional M7061's or to obtain additional high-resolution memory channels, such as two 512x512 pixel by 4-bit Interlaced channels). For VSV11 systems, a backplane (H9273 or equivalent) must be

available to contiguously contain all modules. For VS11 systems, the DDV11-DK 9-slot backplane, shown in Figure 2-29 and included in some of the building blocks listed in Paragraph 2.8.1, is available. In addition, for UNIBUS-based systems, an H9273 backplane can be used if the VS11-BC/BD building block, described in Paragraph 2.8.1 is used.

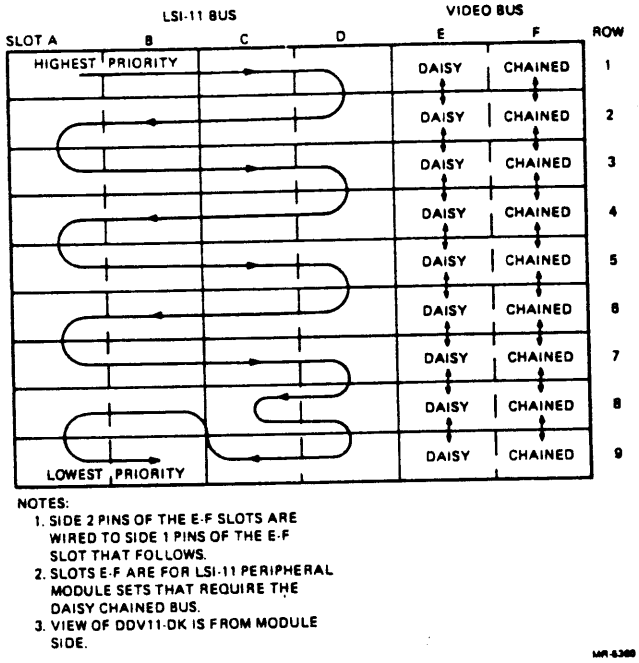


Figure 2-29
DDV11-DK 9-Slot Backplane

2.8.1 Building Blocks

Extended systems are constructed using a "building block" approach. The following building blocks are available (in the model designations, the two variations given, such as -BA/BB, are the same except for switch and jumper settings used to select between 60Hz and 50Hz operation):

VSV11-BA/BB: VSV11-AA/AB plus DDV11-DK 9-Slot Backplane, Power Harness Adapter, Six G7272 Grant Continuity Cards, DBUS Data Cable with 9 Connection Points, and M9403 LSI-11 Bus Connector with +15V to +12V Converter. The VSV11-BA/BB is used when it is desired to use a PDP-11 type mounting box on an LSI-11 Bus system. Additional equipment required would be two BC05L cables and an M9401 Connector to extend the LSI-11 Bus.

VS11-BA/BB: VSV11-AA/AB with DW11-EK UNIBUS to LSI-11 Bus Converter. This is the same as a VS11-AA/AB except that a DDV11-DK 9-Slot Backplane is used rather than the 4-slot DDV11-CK.

VS11-BC/BD: VSV11-AA/AB with DW11-A UNIBUS to LSI-11 Bus Converter. The DW11-A contains an M8217 bus converter module (for installation in a UNIBUS SPC slot), an M9401 LSI-11 Bus Connector module, and two BC05L-16 16-foot 40-Conductor Ribbon Cables to interconnect the M8217 and M9401. This building block is to be used on a PDP-11 system with an LSI-11 expansion box, such as the BA11-N, and H9273-A backplane.

VSV11-MA: M7062 Image Memory Module.

VSV11-SA/SB: M7061 Sync Generator/Cursor Control Module plus Video Cables.

VSV11-SC/SD: M7061 Sync Generator/Cursor Control Module, Video Cables and Joystick Pigtail Cable.

VSV11-SE/SF: M7061 Sync Generator/Cursor Control Module, Video Cables, and Multi-Tap Joystick Pigtail Cable (for connecting a single H3060 Joystick to up to four M7061 modules).

VSV11-SH: M7061 Sync Generator/Cursor Control Module.

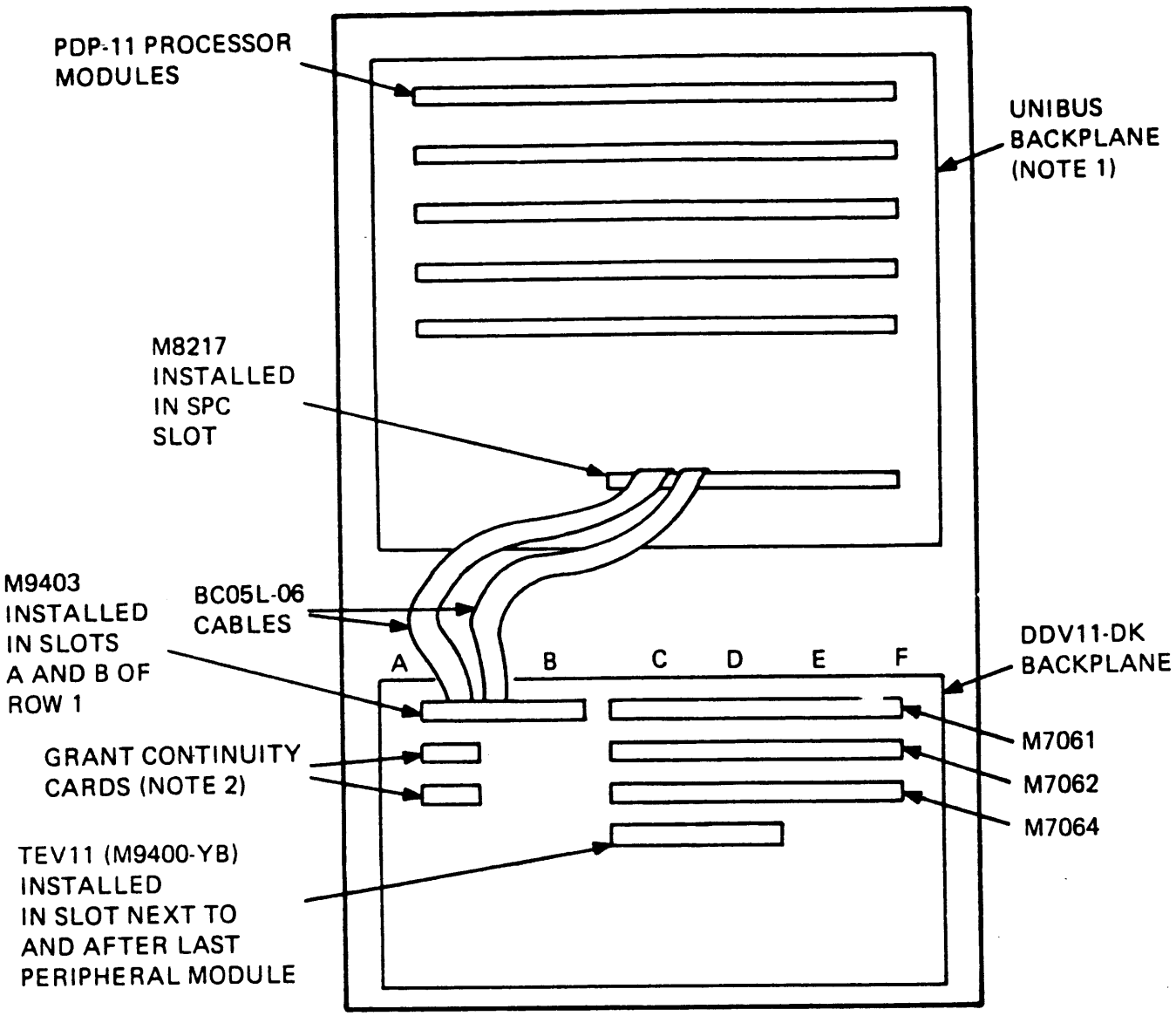
H3060: Joystick Assembly.

VT100-LA/LB: Monochrome Monitor Terminal.

VRV02-AA/AB: 19-inch Color Monitor (no Keyboard or terminal logic).

VRV02-BA/BB: 19-inch Color Monitor Terminal (with Keyboard).

Notice that the VSV11/VS11-Bx series of building blocks are nothing more than a basic VSV11-AA/AB for use with a larger backplane. Therefore, the VSV11/VS11-Bx option should first be installed, using the procedures given in Paragraphs 2.1 through 2.7. Figure 2-30 illustrates the VS11-BA/BB installation. If two M7062 Image Memory modules are to be installed in the first memory channel, include the second memory (VSV11-MA) during basic installation (Figure 2-31). Following basic installation, additional Memory and Joystick channels can be added to obtain the extended configurations described in Paragraph 2.8.2.

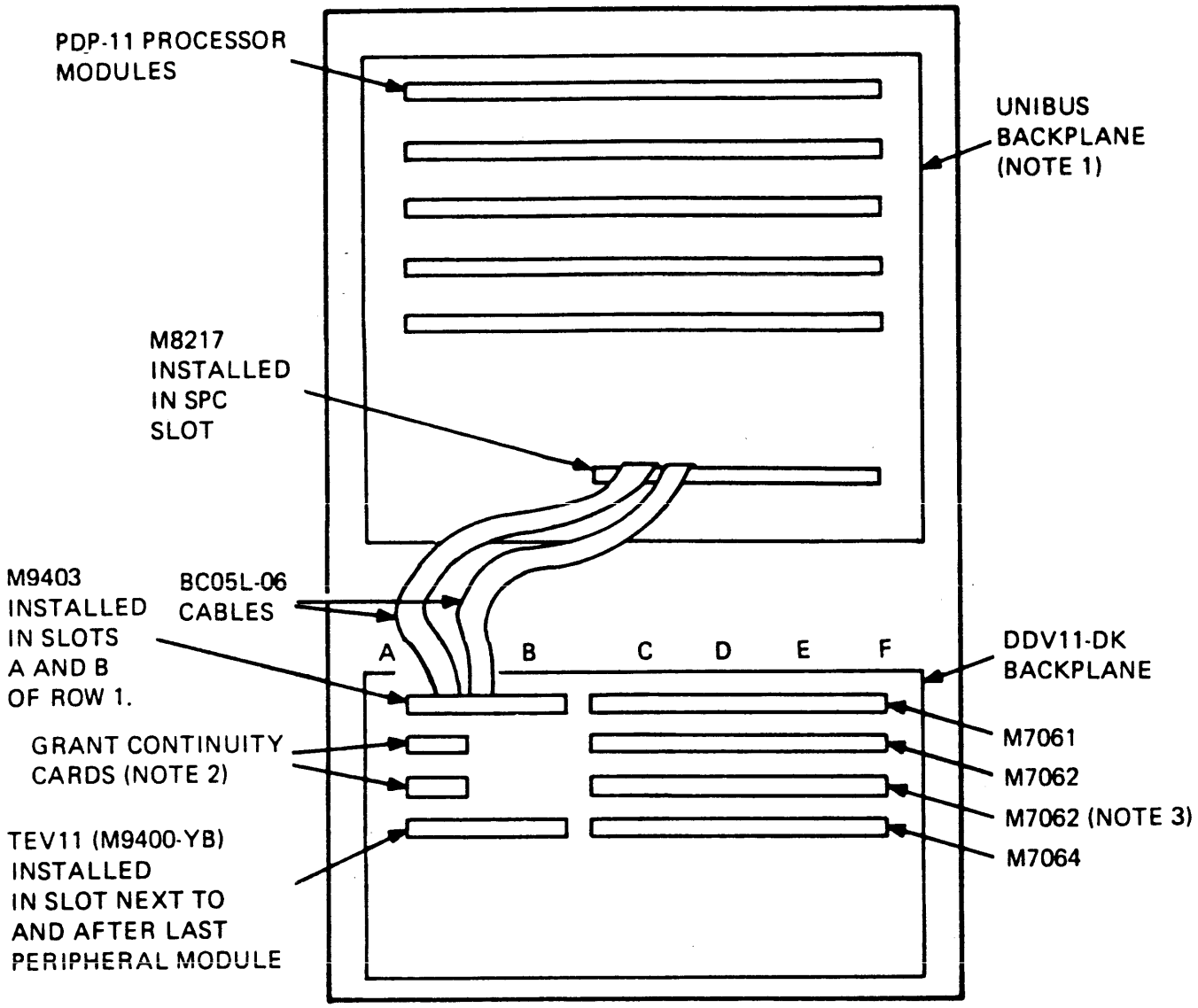


NOTES:

1. IF UNIBUS BACKPLANE IS A DD11-B, -C, -D, OR -P, THE BACKPLANE MUST BE AT THE PROPER REVISION LEVEL.
2. IF THESE SLOTS ARE UNUSED, G7272 GRANT CONTINUITY CARDS MUST BE INSTALLED HERE.

MR-5361

Figure 2-30
VS11-BA/BB Installation Configuration



NOTES:

1. IF UNIBUS BACKPLANE IS A DD11-B, -C, -D, OR -P, THE BACKPLANE MUST BE AT THE PROPER REVISION LEVEL.
2. IF THESE SLOTS ARE UNUSED, G7272 GRANT CONTINUITY CARDS MUST BE INSTALLED HERE.
3. REMOVE THE TERMINATOR RESISTOR PACKS FROM THIS M7062.

MR-5362

Figure 2-31
VS11-BA/BB w/VSV11-MA Installation Configuration

2.8.2 Installation Of Extensions

Additional M7062 Image Memory and M7061 Sync Generator components can be used in a variety of ways. For example, the block diagram of Figure 2-32 illustrates a VSV11 system configured to drive two independent monitors. Figure 2-33 shows the physical module arrangement for the two-monitor configuration of Figure 2-32. In such a system, only one of the monitors can be operated in the External Sync mode (necessary for VT100-LA/LB operation, and for use of VRV02-BA/BB as a terminal, with keyboard data on the screen) since only one M7061 module (termed the Master) can provide timing for the entire VSV11 system.

The structure of the backplanes used in the VSV11/VS11 systems is such that the video data supplied by M7062 Image Memories is isolated by an intervening M7061 Sync module. For example, if M7061 Sync modules are installed in rows 1 and 3 of a DDV11-DK backplane and M7061 Image Memory modules are installed in rows 2 and 4, the memory in row 2 supplies data only to the M7061 in row 1, and the memory in row 4 supplies data only to the M7062 in row 3. This fact allows the installation procedure to be handled on an M7061-by-M7061 basis, with M7062 Image Memories allocated as required. The entire system, however, must be either Interlaced or Non-Interlaced since the first M7061 controls the timing and operating mode of all other units.

There can be a maximum of 4 Image Memory channels and 4 M7061 channels on a VSV11/VS11 system. Each memory channel can contain either one or two M7062 Image Memory modules. If two M7062 modules are used in any memory channel, the system must be configured in the Interlaced mode, providing 512x512 pixels by 4 bits of data (each module handles two bits of data). Therefore, the following configurations can be obtained (given that space and power are available):

1. Four M7061's (Sync Channels 0 through 3), each supplied by one memory channel (Memory Channels 0 through 3, respectively). Each memory channel can contain 1 M7062 (Interlaced or Non-Interlaced system) or 2 M7062's (Interlaced system only).

2. One M7061 (Sync Channel 0), with 4 memory channels (Channels 0 through 3), with each memory channel containing 1 or 2 M7062 modules.

3. Two M7061's (Sync Channels 0 and 1) each containing 2 memory channels (Memory Channels 0 and 1 on Sync Channel 0, Memory Channels 2 and 3 on Sync Channel 1).

4. Two M7061's (Sync Channels 0 and 1), with one memory channel on one Sync channel and 2 or 3 memory channels on the other Sync channel.

5. Three M7061's (Sync Channels 0 through 2), with one memory channel on each Sync channel or one memory channel on two of the Sync channels and two memory channels on the third.

When installing complex extended configurations, it is recommended that the system be decomposed into single Sync/Memory groups, corresponding to one of the standard VSV11/VS11 3- or 4-slot configurations; each group can then be installed and tested separately using the proceedures described in the preceeding paragraphs. For example, a system with two M7061 Sync modules and two M7062 Memory modules could be installed by handling each Sync/Memory combination as a VSV11/VS11-AA, -AB, -AE, -AF, -AP, or -AR. After installing and testing one combination, remove it and install and test the other. Finally, move the M7064 Display Processor module over two rows in the backplane, configure the second Sync module for Channel 1 and Slave operation (Table 2-13) and its companion Memory module for Channel 1 (Table 2-14 or 2-15). Install the second combination and check out the entire system using the diagnostic. Be sure to run Test 35, the Configuration Typeout test, and verify that the appropriate configuration is present.

In all installations, the following guidelines should be observed:

1. If multiple M7061 Sync Generator modules are being used, only one can be set for Master operation (switch E21-6 ON and jumper W19 IN); all other M7061's must be in the Slave mode (E21-6 OFF and jumper W19 OUT). In addition, for ease of maintenance, the Master M7061 should be configured as Channel 0 and should be the module furthest away from the M7064. (The Master M7061 should be in the lowest-numbered backplane row).

2. When assigning channel numbers to multiple Sync and Memory modules, the lowest-numbered channels should be assigned to the modules in the lowest-numbered backplane rows; the highest-numbered channels should be nearest the M7064 Display Processor module.

3. The M7062 Memory module in the lowest-numbered backplane row (nearest the Master Sync module) should have resistor packs installed in I.C. locations E76 and E77; all other memory modules should have the resistor packs removed.

4. If two M7062 memory modules per memory channel are used (Interlaced operation), the module handling the most-significant pixel bits (switches 3 and 4 on E49 and E59 ON) should be in the lowest-numbered backplane row.

A general installation can be performed as follows (be sure to refer to the guidelines given previously):

1. Unpack all components and inventory them against the VSV11 or VS11 Field Maintenance Print Set.

2. Inspect the computer system and verify that appropriate space and power are available. Refer to Chapter 1 of the VSV11/VS11 Option Description and sum the dc power requirements of the logic modules; the sum cannot exceed the power supplied by the mounting box. For VS11 systems, +15Vdc current is required equivalent to the +12Vdc current listed for the M7062 and M7061 modules.

3. Install the basic VSV11 or VS11 hardware (i.e., the minimal configuration with one Memory channel and one Sync/Joystick channel) using the procedures of Paragraphs 2.2 through 2.7.

4. Prepare any additional display monitors (refer to Paragraph 2.3). If multiple monitors are to be attached to a single M7061, only the last monitor in the string must be terminated in 75 ohms. For example, if two VRV02's are used on the same channel, the first one must have the 75-OHM/HIGH toggle switch on the rear of the cabinet in the HIGH position (down); the last one must have the switch in the 75-OHM position (up).

5. Configure the switches and jumpers on each additional M7062 Image Memory and M7061 module, carefully assigning the channel numbers and functionality. Note especially that all M7062 Image Memory modules must be configured to run in the same mode (Interlaced or Non-Interlaced) and that additional M7061 modules must be configured as Slaves (sync generation logic disabled). For the M7061, refer to Table 2-13. For the M7062, refer to Tables 2-14 or 2-15.

6. Install and check out the additional modules, cables, monitors and joysticks one channel at a time.

7. Check out and accept the system using the supplied diagnostic program.

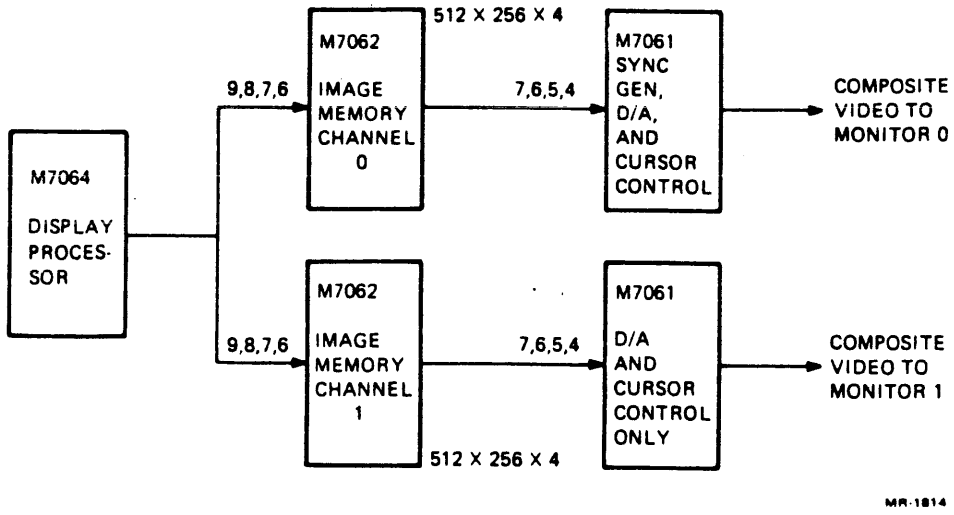


Figure 2-32
VSV11 System w/ Two Independent Monitors

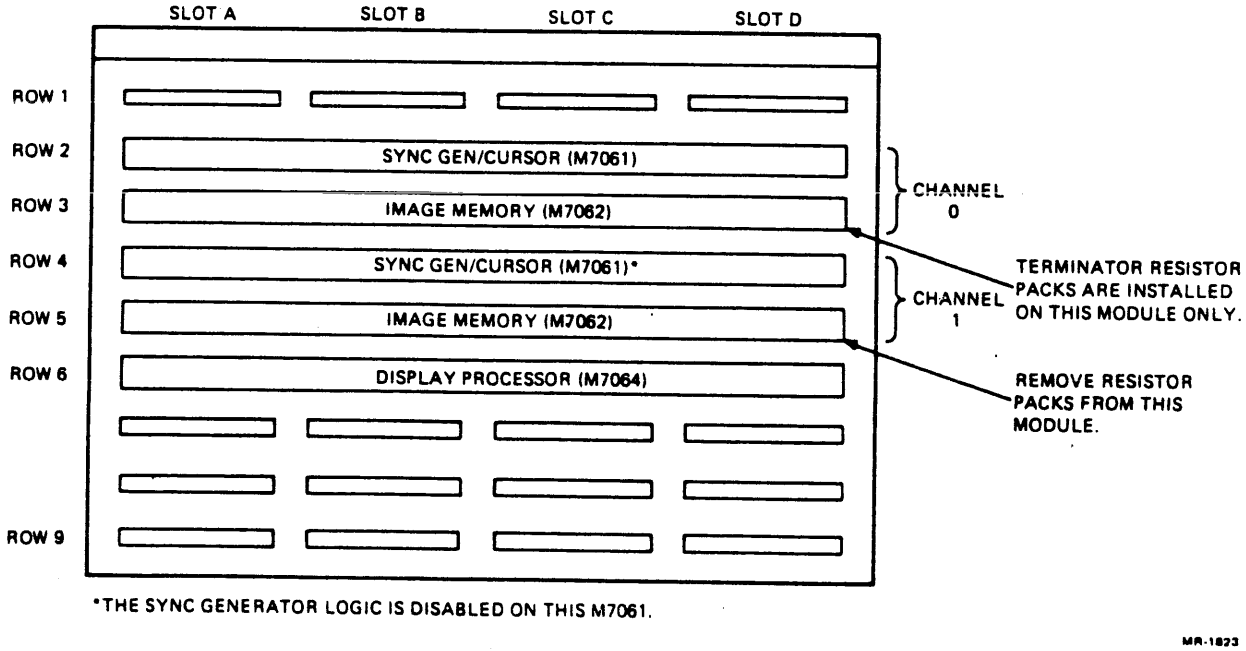


Figure 2-33
Module Arrangement for 2-Monitor System

CHAPTER 3

PROGRAMMING REFERENCE

3.1 INTRODUCTION

This chapter presents machine-level programming information for the VSV11/VS11 graphic system. The discussion presented assumes the VSV11/VS11 programmer has prior programming experience in graphics. Therefore, the programming information presented here is a machine-level programmer's reference rather than an application programming reference. Topics discussed include the VSV11/VS11 programming concept, bus addressable registers, system interrupts, the VSV11/VS11 instruction set, and the make-up of a CPU memory display file.

3.2 VSV11/VS11 PROGRAMMING CONCEPT

Data to be displayed by the VSV11/VS11 is first organized into a display file in the memory of the host CPU. This file consists of a series of VSV11/VS11 instructions (graphic, control, and data instructions) which define an image. In essence, the display file is a program written in the VSV11/VS11 machine language. After the display file is constructed, the VSV11/VS11 display "program" is initiated by moving the display file starting address to the VSV11/VS11 Display Program Counter (DPC). Once initiated, the VSV11/VS11 issues Non-Processor Requests (NPR's) to sequence through the display file instructions and generate the desired image on the system monitor. Since the VSV11/VS11 contains an Image Memory, continuous image refresh from CPU memory is not required. After one pass through the memory file, the file may be altered or removed.

Pictures are produced by writing pixel data into one or more image memories. The memories to be written must be enabled for writing by the program via a control instruction and, since more than one memory can be write-enabled at a time, the program must also assure that memories not to be written are placed in a Read-Only or Protect state. Once the graphic data is written, the program must assure that the memory is placed in a Read-Only or Read/Write state so the pixel data is "read out" to the monitor. Image memories feed data to a Sync Generator/Cursor

Control module (termed a "Sync/Joystick Channel) for display on a monitor. There can be up to four memory channels and four Sync/Joystick channels. A Sync/Joystick channel can be associated with one, two, three or four memories; it is the responsibility of the display programmer to know the system configuration so that memory and Sync/Joystick operations are coordinated. The image memories have an "edge detect" circuit so that data written to coordinates beyond the visible screen area does not "wrap around"; data will not wrap around until 12 bits of position, in the 1024-point format, are exceeded (the visible area is accessed with up to 10 bits of coordinate data, but the least-significant bit is not used).

3.3 VSV11/VS11 ADDRESSABLE REGISTERS

The VSV11/VS11 has four device registers which can be addressed for read/write transfers from the LSI-11 Bus. These registers are listed in Table 3-1, along with their standard factory addresses.

Table 3-1
VSV11/VS11 Addressable Registers

Register Name	Factory Bus Address (Octal)
Display Program Counter (DPC)	772010
Display Status Register (DSR)	772012
Display X Status Register (DXR)	772014
Display Y Status Register (DYR)	772016

Data can be read from or written into these registers only when the VSV11/VS11 Display Processor (abbreviated DP or DPU) is in the internal stop (IDLE) condition (bit 15 of the DSR register set). An attempted write to any of these registers while the Display Processor is running will cause the Display Processor to halt after completion of the display instruction that is currently being processed. Reading any of these registers while the Display Processor is not stopped results in read-back data of all zeros.

The address of the device register block can be switch-selected to begin on any 4-word boundary in the I/O register page. The general register address specifications will therefore be given as 7xxxx0 through 7xxxx6 in the following paragraphs.

In the discussions which follow, the term "Initialize" refers to the occurrence of the Bus-INIT signal and to the "Soft Initialize" function performed when 100000 (octal) is written into the DYR register (Paragraph 3.3.4). During the initialization sequence, various internal registers are cleared

or set to known states, pending interrupts ar the Graphic Mode is cleared to Character mode, the Joystick and Cursor Match interrupt enables are cleared, the intensity is turned off, and all image memory channels are set tc the Write-Only mode and the image memories are cleared. In addition, a self-test sequence is performed in which the DBUS Data lines are checked and the state of various status signals verified. If a problem is detected, the appropriate error code is loaded into the CSR register (Paragraph 3.3.2.4) and the Idle state is entered directly without clearing the Sync/Joystick channels or image memories. The initialization sequence lasts approximately 40 milliseconds, during which time the Display Processor registers are not accessible. Therefore, the program must wait for the STOP bit in DSR to appear before attempting any operations with the VSV11/VS11. After the STOP bit appears, it is recommended that the CSR be checked for any errors before proceeding.

3.3.1 Display Program Counter (DPC) 7xxxx0

The Display Program Counter (DPC), shown in Figure 3-1, contains the virtual address of the next host memory location to be addressed by the VSV11 Display Processor. It can be read and written at the general address 7xxxx0. The DPC contains a 16-bit number representing the address of a word within the user's display file; internally, the DPC holds a memory byte address with bit 0 always 0 (the VSV11 addresses host memory on a word basis only).

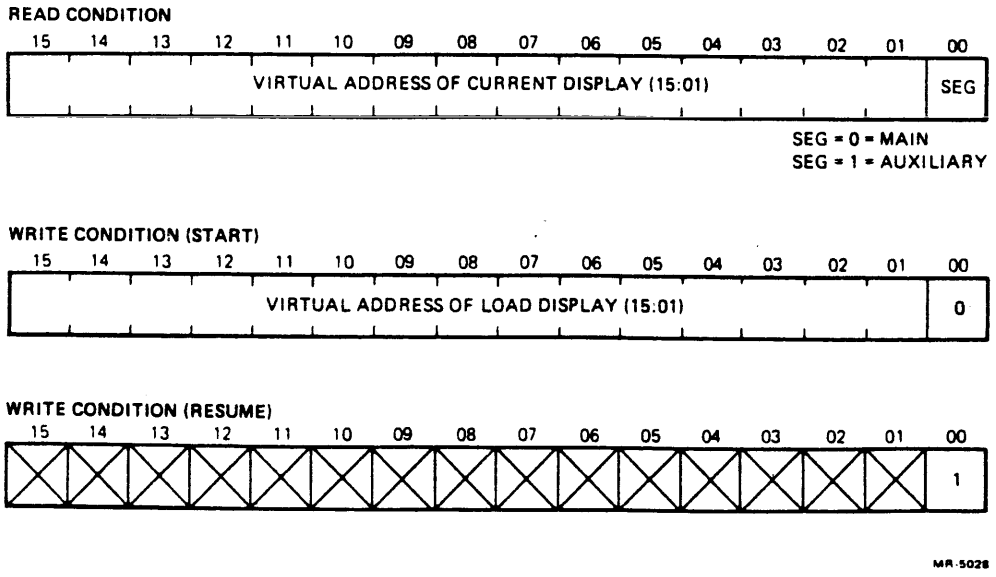


Figure 3-1
Display Program Counter (DPC)

The 16-bit DPC can only reference up to 32K words of memory, since it can generate addresses only in the range 0-177776. In order to allow the display file to be placed anywhere within the 128K-word bus address space (using 18-bit addresses), the content of DPC is not used as a direct physical address. Rather, the virtual address in DPC is added to a Relocation value to yield an 18-bit physical address. The relocation structure used in the VSV11, described in Paragraph 3.3.2.5, allows a display file to start (virtual DPC=0) on any 32-word boundary in physical memory; this is consistent with the relocation resolution of the memory mapping mechanism of the PDP-11.

The VSV11/VS11 also has the ability to limit the range of DPC addressing to an area less an 32K words. Limits can be set for 2K, 4K, 8K, or 16K words, under control of a Protection Mask. In addition, a bit can be set to inhibit the DPU from writing into memory when a DMA Pixel Readback instruction is encountered. The Relocation value, Protection Mask, and Write-Protect bit are collectively termed the "memory management" parameters. These are described in Paragraphs 3.3.2.5 through 3.3.2.8.

The virtual area that the DPC can address is termed a "segment". The VSV11 supports up to two such segments, termed Main and Auxiliary. Each is associated with its own set of memory-management parameters (4-bit protection mask, 1-bit write-protect, and 12-bit relocation value). Normally, the Display Processor executes display instructions from the Main segment. The Auxiliary segment can be used for display subroutines (called via the CHARACTER or DJMS instructions) and for Bit Map data. The DPOP instruction returns the display program to the Main segment at the end of a subroutine.

Figure 3-1 depicts the format of the DPC for reading and writing. When read, bits 1-15 display the virtual address of the next display word to be executed; bit 0 indicates the current segment being accessed (0 = MAIN, 1 = AUXILIARY). DPC (and all other VSV11 registers) are only accessible when the Display Processor is "idle"" (stopped). If a register is read while the Processor is "busy" (executing the display file or performing operations such as Pixel Readback or Cursor Readback), all 0's are returned. DSR Bit 15 (STOP) can be monitored to determine the state of the processor.

When DPC is written (with the processor not busy), One of two actions, START or RESUME, is taken depending upon the data written into bit 0. If bit 0 is written to 0, a START sequence is initiated, causing the following:

1. The written data is loaded into the internal DPC register, becoming the new display file virtual address.

2. The internal "Current Segment" flag is cleared, selecting the Main segment.

3. The internal "Processing Character" flag is cleared, forcing a new character data word to be fetched if the processor is presently in Character Mode and a data word is the first display file item fetched.

4. Bit 0 of the PCSAVE register (Paragraph 3.3.2.2) is set, indicating that it is "empty" and is available for use during subroutines and Bit Map modes. [000001 is loaded into PCSAVE]

   [RESUME starts here]

5. The processor becomes "busy" (stop bit is cleared).

6. The internal DSR-location Register Select code (Paragraph 3.3.2) is cleared to 0, selecting the actual DSR register; this facilitates monitoring of the STOP bit. Pending interrupts are also cleared.

7. The "working" memory-management registers are loaded with the parameters stored in MAINMM or AUXMM (Paragraphs 3.3.2.5 through 3.3.2.8), depending upon the state of the "Current Segment" flag (on a START, the parameters for the Main segment will always be used).

8. Display processing commences with a dispatch to the current graphic-mode instruction, which fetches the word addressed by the virtual address in DPC.

If bit 0 of DPC is written to 1, a RESUME sequence is initiated. Bits 1-15 of the data are ignored, leaving the current DPC intact. The sequence begins at Step 5 above. Note that the Current Segment and Character Processing flags are left intact.

DPC is cleared by Initialize (bus INIT signal or programmed initialize).

3.3.2 Display Status Register (DSR) 7xxxx2

The DSR bus location, at general address 7xxxx2, serves as a data "pathway" to several internal VSV11 registers. The particular internal register to be read or written is selected by writing a selection code into bits 2-0 of the DSR location. The register is written by writing into DSR a word that has the selection code in bits 2-0, bit 3 set to 1 (Write-Enable), and bits 15-4 containing the register-specific data to be written. A register is read by first writing the selection code and then reading DSR to obtain the data. Note that writing DSR with bit 3=0 (no write-enable) sets the selection code and causes no data to be written.

Table 3-2 lists the DSR selection codes. Each of the selectable registers is described in the following paragraphs.

Table 3-2
DSR Selection Codes

DSR<2:0> CODE	WRITE	READ
0	---	DSR (Display Status: Op-code, Pixel Data, and Stop Bit)
1	Unused	PCSAVE (DPC for subroutine return)
2	FLAGS (Clear pending interrupts and joystick lockout)	FLAGS (Pending interrupts, Joystick Lockout and current Graphic-Mode Op-code)
3	CSR (Control-Status)	CSR (Control-Status)
4	Main-Segment Relocation	MAINMM (Main Mem. Mgmt.)
5	Main-Segment Protection	HBASE (Histogram Base & segment write-protection
6	Auxiliary-Segment Relocation	AUXMM (Aux Mem. Mgmt.)
7	Auxiliary-Segment Protection	CBASE (Character Base)

The Selection code (stored internally) is cleared to 0 whenever the Display Processor becomes "busy" (i.e., on any write to the DPC, DXR or DYR registers, for a START, RESUME, PIXEL READBACK, WRITE JOYSTICK STATUS REGISTER etc.) to facilitate program interaction with the STOP flag of DSR.

3.3.2.1 DSR (Display Status) [Select = 0] -

The internal DSR register (Figure 3-2) holds Pixel Data, Instruction Op-code, and the STOP flag; these fields are described in Table 3-3. Writing DSR with 0 selects the internal ("real") DSR. The DSR itself is read-only; it cannot be written.

NOTE

On a STOP following execution of the DMA Pixel Readback display instruction, the DSR contains the entire instruction word; the current pixel data field, DSR <9:0>, is not preserved.

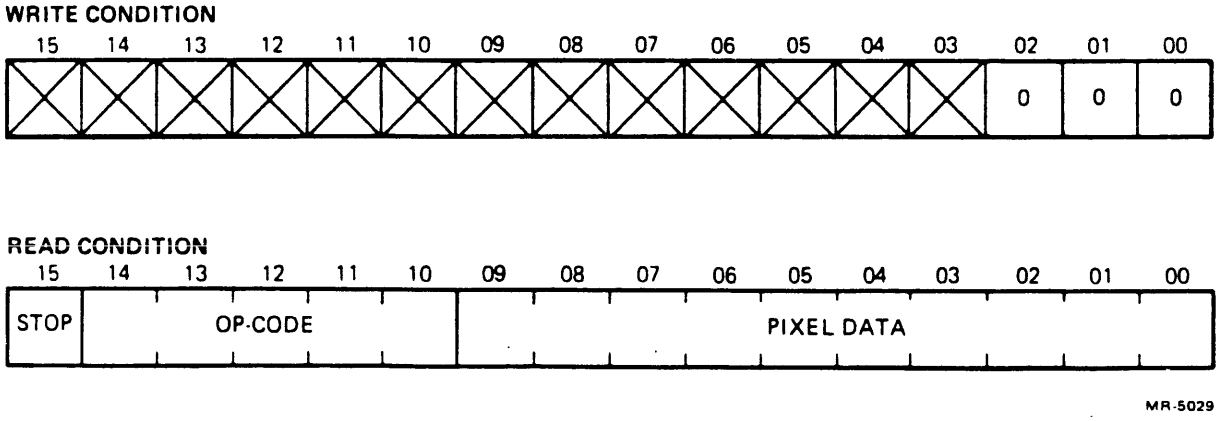


Figure 3-2
DSR Register Bit Configuration

Table 3-3
DSR Register Bit Definitions

Bit	Name	Description
15	STOP Flag	When set, indicates that the Display Processor is in the stopped or "IDLE" state (registers can be read and written).
14-10	OP-CODE	Current Instruction Op-code (bits 10-14 of the last instruction word fetched from the display file).
9-0	Pixel Data	Current Pixel Data (bits 0-9 of the last Graphic Mode instruction fetched from the display file), or contents of the image memory at a specified X,Y location returned from the Pixel Readback operation (Paragraphs 3.3.3 and 3.3.4, DXR & DYR descriptions, for Pixel Readback procedure). After execution of a DMA Pixel Readback instruction, bits 9-1 of this field contain bits 9-1 of the first instruction word; bit 0 contains the "incomplete" flag (Paragraph 3.5.3.3).

3.3.2.2 PCSAVE (Saved DPC From Subroutine) [Select = 1] -

Writing a 1 into the DSR bus location selects the PCSAVE register for reading. The register format is shown in Figure 3-3.

The Display Processor implements a limited display subroutine capability, allowing "subpicture" routines to be called from the main display file program. Such subroutines are called with the CHARACTER Graphic Mode instruction and with the DJMS (Display Jump-to-Subroutine) instruction. The "return address" (to get back to the main display program with a DPOP instruction) is stored in PCSAVE. PCSAVE therefore contains the virtual address of the next element to be fetched from the main display file. Bit 0 of PCSAVE is the "empty" indication:

PCSAVE<0>=0: Full. A subroutine is not allowed to be called, since the processor is already in one.

PCSAVE<0>=1: Empty. A subroutine is allowed to be called.

Note that subroutines cannot be called from the auxiliary segment. PCSAVE is also used during processing of Bit-Map and DMA Pixel Readback instructions to save the display file address when the DPC is used for the data "dispatch" address, so one of these instructions cannot be used within a subroutine.

PCSAVE is set to 000001 (empty) by Initialize.

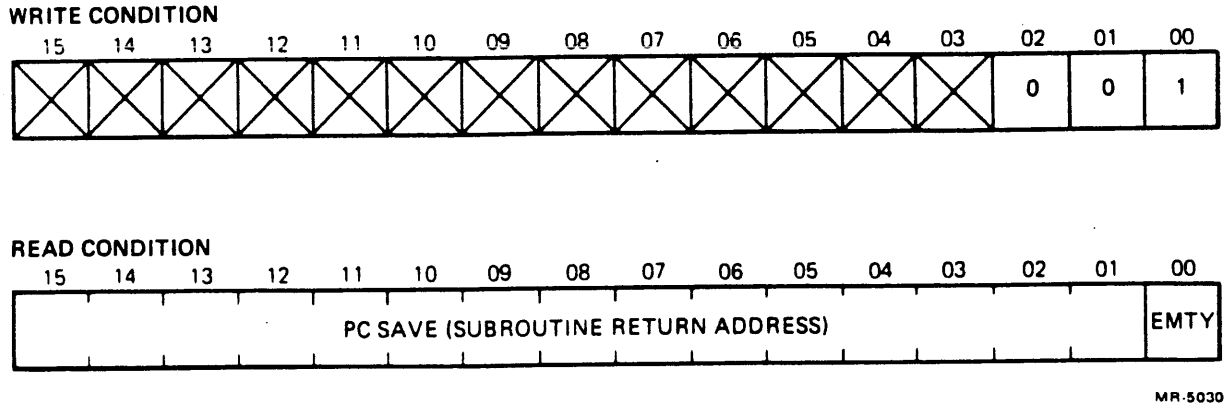


Figure 3-3
PCSAVE/DSR-SELECT=1 Register Configuration

3.3.2.3 FLAGS (Pending Interrupts & Graphic Mode) [Select=2] -

Writing a 2 into the DSR bus location selects the internal FLAGS register for reading. The contents of FLAGS displays the current Graphic Mode and indicates the presence of interrupt requests issued by the Display Processor. Writing a 12 (Write-Enable + SELECT CODE 2) into the DSR location clears all pending interrupts. Pending interrupts and flags are also cleared by a START or RESUME (Paragraph 3.3.1). Figure 3-4 shows the format of FLAGS. Table 3-4 describes each bit.

The flags and Graphic Mode are cleared by Initialize.

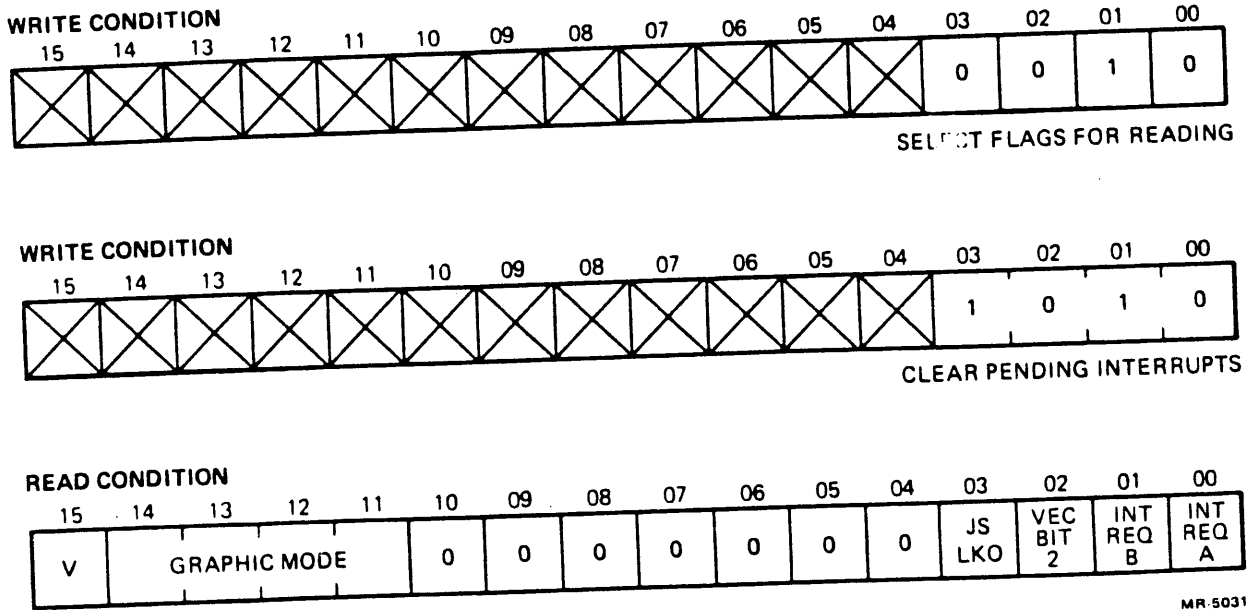


Figure 3-4
FLAGS/DSR-SELECT=2 Register Configuration

Table 3-4
FLAGS Register Bit Definitions

Bit	Name	Description
15	"Valid" Flag	=1 if bits 14-11 contain a valid representation of the current Graphic Mode.
14-11	Graphic Mode	Op-code (Bits 14-11) of the last Graphic Mode instruction fetched from the display file.
10-4	Unused	Always read as 0.
3	JS LKO	Joystick Lockout. Set to 1 when the Joystick Switch Interrupt (JSSWI) condition (from the currently selected SYNC module) is recognized by the DPU in the Idle state; INT REQ B and VEC BIT 2 are also set at this time in order to post the interrupt. JSSWI is only recognized if all of bits FLAGS<3:0> are clear. Therefore, the programmer must write into FLAGS if more than one JSSWI interrupt must be detected. This action allows time for the program to read the Cursor coordinates.
2	VEC BIT 2	Vector Bit 2 for INT REQ A or B
1	INT REQ B	Request pending on Channel B. If VEC BIT 2=0, ERROR interrupt is pending. If VEC BIT 2=1, JOYSTICK SWITCH interrupt is pending.
0	INT REQ A	Request pending on Channel A. If VEC BIT 2=0, a STOP interrupt is pending. If VEC BIT 2=1, a CURSOR MATCH interrupt is pending.

NOTE

INT REQ A and INT REQ B are mutually exclusive; only one interrupt may be pending at any one time.

3.3.2.4 CSR (Control-Status Register)[Select=3](Read/Write) -

Writing 3 into bits 2-0 of the DSR bus location selects the CSR for reading (bit 3=0) or writing/reading (bit 3=1). Figure 3-5 shows the format of CSR and Table 3-5 describes each bit.

The CSR is cleared by Initialize.

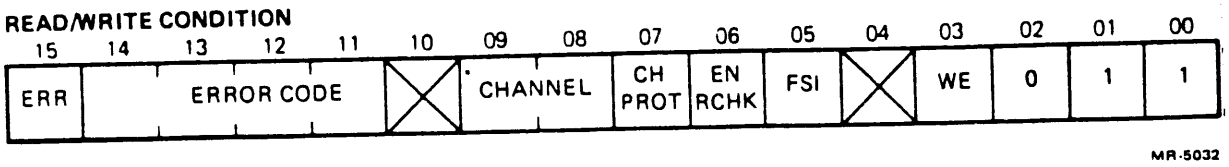


Figure 3-5
CSR Register Configuration

Table 3-5
CSR Register Bit Definitions

Bit	Name	Description
15	ERR (Composite Error Flag)	ERR is the inclusive-OR of all error code bits (bits 11-14). It is set when the Display Processor sets an error code. All errors cause display processing to stop.
14-11	Error Code	Set by the DPU/TO indicate the type of error encountered, as detailed in Table 3-6.
10	Spare	(Can be written & read, but has no function)
9-8	CHANNEL	If the CH PROT bit is 1, these two bits replace the Channel Select bits of the data sent on the DBUS during the JOYSTICK STATUS, LOAD STATUS C, WRITE EXTENDED JOYSTICK CONTROL, and WRITE CURSOR COORDINATES display instructions.
7	CH PROT (Channel Protect)	If this bit is 0, Image Memory and Joystick channels are selected from the display file, via bits in the JOYSTICK STATUS, LOAD STATUS C, WRITE CURSOR COORDINATES or EXTENDED JOYSTICK CONTROL instructions. If this bit is 1, channel selection is supplied from CSR<9:8>.

Table 3-5 (con't)
CSR Register Bit Definitions

Bit	Name	Description
6	EN RCHK (Enable Reserved Operation Check)	Setting this bit enables the Display Processor to produce the RSVD OP error condition. If this bit is 0, undefined operation codes are treated as NO-OP's and most undefined data fields are ignored. Some specific RSVD OP errors are flagged even if this bit is 0.
5	FSI (Force Stop Interrupt)	Setting this bit assures than an interrupt is requested whenever the Display Processor stops display file processing. This includes a STOP coded into a Status-A instruction regardless of whether the Stop Interrupt was enabled. Not included is the transition from "busy" to "idle" at the end of functions performed by writing into the DXR or DYR registers (e.g., Pixel Readback and "Soft Initialize"). (See descriptions of the DXR and DYR registers).
4	Spare	(Can be written & read, but has no function)
3	WE (Write Enable)	A 1 must be written into this bit to cause bits 4-15 of the CSR to be written. If a 0 is written into WE, only the internal register selection code is changed, allowing the selected register to be subsequently read.
2-0	Selection Code	The DSR register selection code is stored internally in bits 2-0 of the CSR scratchpad register. So, these bits will always have the CSR selection code (011) when CSR is accessed.

Table 3-6
CSR Error Codes

Code	Name	Description
1 =0001	NXM (Nonexistent Memory Error)	Set by the Display Processor to indicate that, during a DMA cycle, a memory location was addressed but no response was received within 10 microseconds.
3 =0011	MPE (Memory Protection Error)	Set by the Display Processor to indicate that the virtual address in DPC is out of range. The DPC is tested against the protection mask before each DMA cycle; if any bits in DPC are set (1) corresponding to bits set in the mask, MPE and ERR are set, display processing stops and the ERROR interrupt is requested. The MPE error also occurs if, during the DMA Pixel Readback instruction, the data address is in a write- protected segment.
5 =0101	RSVD OP (Reserved Operation Error)	Set by the Display Processor to indicate that one of the undefined (unused) operation codes was fetched and decoded, or that an unused field in certain instructions was nonzero. Checking of reserved operation errors is done only if EN RCHK = 1.
4 =0100	SEQ ERR (Sequence Error)	Set by the Display Processor to indicate a programming inconsistency, such as encountering a CHARACTER instruction while already processing a character subpicture.
6 =0110	Vector "Endpoint" Mismatch Error	Set to indicate that the X-Y endpoint reached after the DPU draws a vector does not equal the X-Y coordinates computed from the Delta parameters before the vector is drawn. This error usually indicates a DPU problem in the 2901 carry or shift logic.

Table 3-6 (con't)
CSR Error Codes

Code	Name	Description
7 =0111	Unused Microword Error	Set to indicate that the DPU executed an unused location in the microcode. (Indicates a microprogram sequencer problem).
10 =1000	Sync Timeout (from Image Memory)	Set to indicate that sync was not received from Image Memory while the DPU was preparing to write into the memory. Indicates that either no memory was write-enabled or that the selected memory is malfunctioning.
11 =1001	DATA AVAILABLE Timeout (Pixel Readback)	Set when DATA AVAILABLE is not received from Image Memory while the DPU is performing a Pixel Readback.
12 =1010	DATA READY Timeout (Joystick Status)	Set when DATA READY is not received from the selected sync module while the DPU is trying to read or write the cursor coordinates. Indicates a malfunctioning or nonexistent sync module.
13 =1011	DBUS DATA Read/Write Error	Set to indicate that, during self-test, the DPU transmitted a data pattern onto the DBUS but did not read back the same pattern. Indicates a problem with either the DPU's DBUS drivers or receivers or with a sync or memory board transmitting illegally. [After stop, DXR = expected data, DYR = actual data.]
14 =1100	DBUS Signal Hung	Set during self-test and several other operations to indicate that one of the DBUS status signals is hung (asserted illegally by a sync or memory board).
15 =1101	VBUS (Video Bus) Signal Hung	Set during self-test and several other operations to indicate that a VBUS status signal is hung.
=0000 =1110 =1111	Spare Error Codes	

3.3.2.5 Main-Segment Relocation/Memory Management [Select=4] -

Selecting register 4 in the DSR bus location allows the Main-Segment Relocation parameter to be written (if bit 3 is written to 1), and the entire Main-Segment Memory Management register (Relocation and Protection Mask) to be read back. Figure 3-6 depicts the register formats for writing and reading.

A 12-bit relocation value (MR<17:6>) is specified by writing into the DSR location with bits 3-0 configured as "1100" (octal 14). This value, stored internally in bits 11-0 of the MAINMM register, is justified and added to the DPC contents to produce a physical memory address during each DMA cycle. Figure 3-7 depicts the relocation process.

The relocation value (and protection mask and Write-Protect bit) is cleared by Initialize, causing the the DPC to reference physical addresses in the range 0 - 32K words.

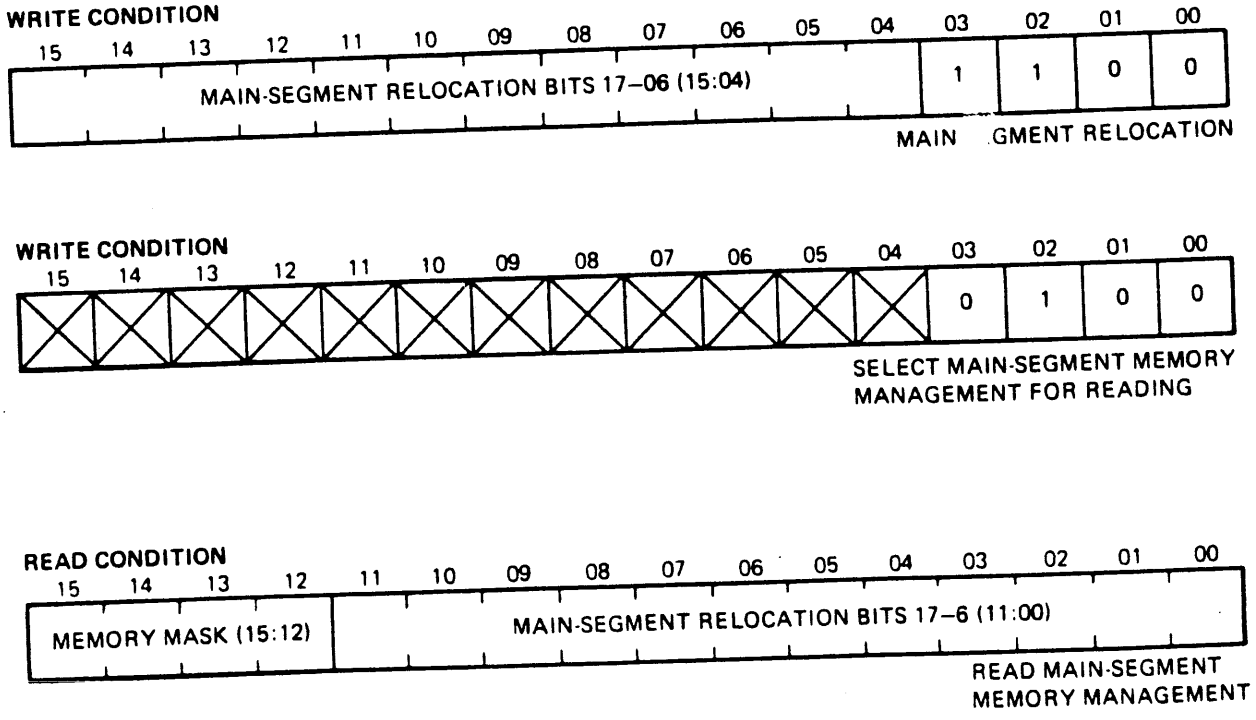


Figure 3-6
Main-Segment Relocation/Memory-Management
Register Format

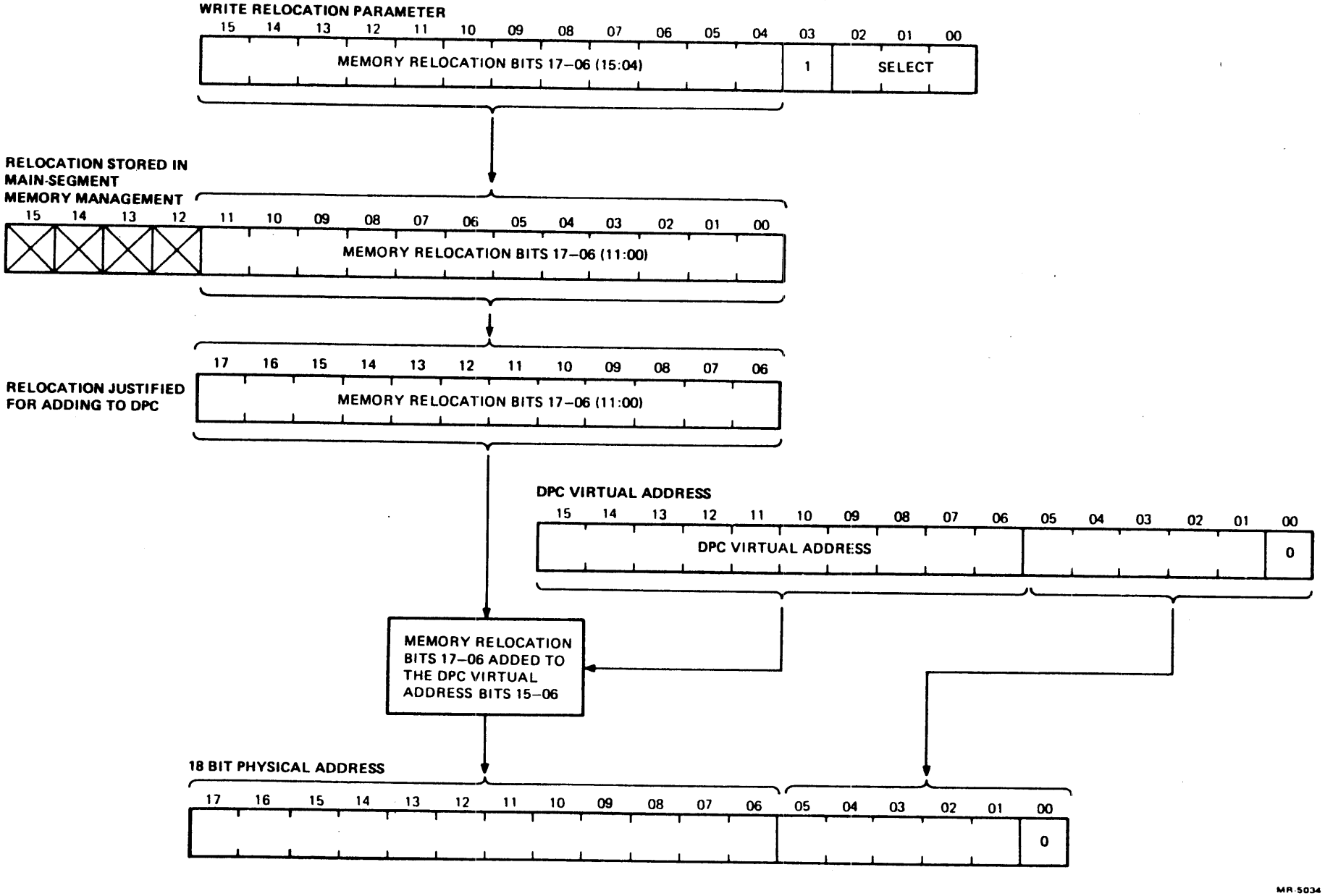


Figure 3-7
Virtual-to-Physical Memory Relocation Process

3.3.2.6 Main-Segment Protection Mask/HBASE Read [select=5] -

Selecting register 5 in the DSR bus location allows the 4-bit Main-Segment Memory-Protection Mask and the Write-Protection bit to be written and the HBASE (Histogram Base) Register to be read. Figure 3-8 depicts the register formats for writing and reading.

The 4-bit Main-Segment Protection Mask parameter (MM<15:12>) is specified by writing into the DSR location with bits 3-0 configured as 1101 (octal 15=WE + Select 5). The mask value, specified in bits 15-12 of the word, is stored in bits 15-12 of the MAINMM register (which can be read back with Select Code 4). When the Display Processor is executing out of the main display-file segment, this mask value (concatenated with 0's in bits 11-0 in the internal mask register PMASK) is logically ANDed with the virtual address in DPC. If the result is non-zero, the DPC is considered to be out of range, and display processing stops with the MPE error condition. The reasonable settings of the protection mask are given in Table 3-7.

Table 3-7
Protection Mask Settings

MM<15:12>	SEGMENT SIZE (WORDS)	VIRTUAL ADDRESS RANGE (OCTAL)
0000	32K	0-177776
1000	16K	0-077776
1100	8K	0-037776
1110	4K	0-017776
1111	2K	0-007776

Writing a 1 into bit 9 (MWP) write protects the main segment -- data cannot be stored by the DMA Pixel Readback instruction. Writing a 0 into bit 9 clears the main segment write-protect, allowing data to be stored. The main-segment write-protect appears as bit 15 of the HBASE register.

When the DSR location is read after Select Code 5 has been specified, the internal HBASE (Histogram Base) register is obtained. This register contains bits 9-1 of the value loaded with the SET HISTOGRAM BASE instruction shifted right 1 place. Paragraph 3.5.2.4 describes the SET HISTOGRAM BASE instruction.

Bits 15 and 14 of HBASE contain the Main- and Auxiliary- segment Write-Protect bits, respectively.

The Protection Mask and Write-Protect bit are cleared by Initialize, allowing a 32K-word write-enabled Main Segment. The HISTOGRAM BASE register is also cleared by Initialize.

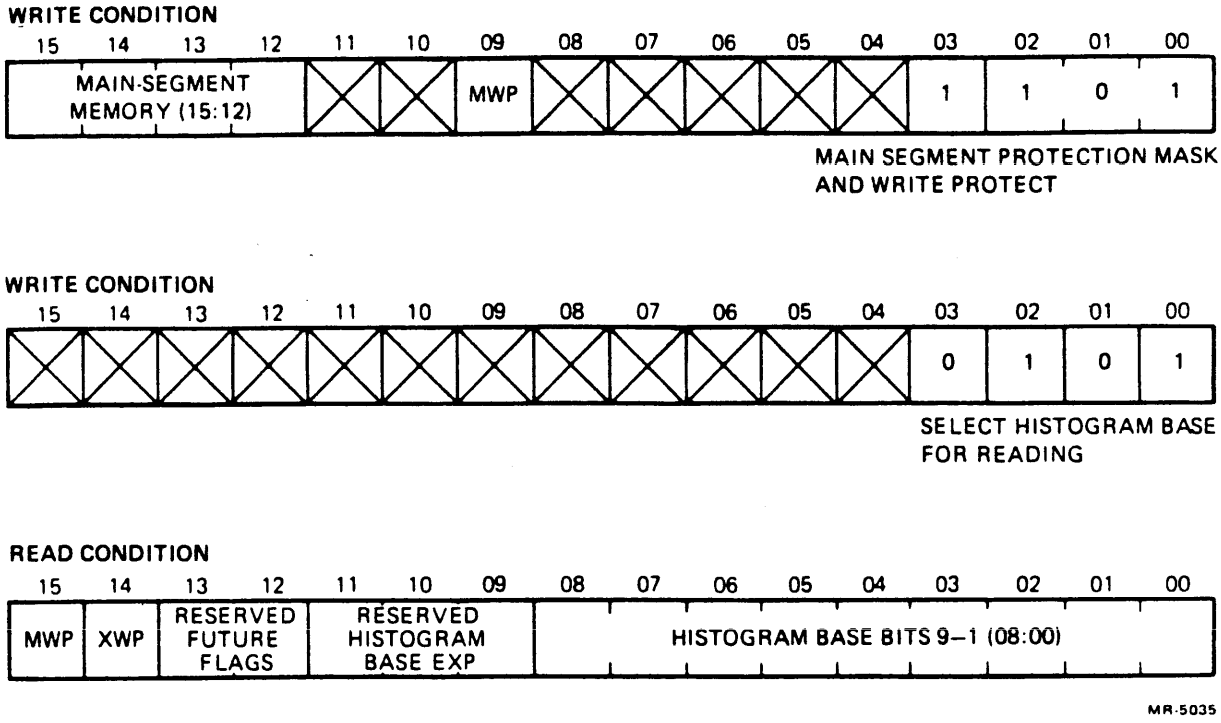


Figure 3-8
DSR Select-Code 5 Register Formats
(Main Segment Mask/HBASE Readback)

3.3.2.7 Auxiliary-Segment Relocation/Memory Mgmt. [Select=6] -

Selecting register 6 in the DSR bus location allows writing of the Auxiliary-Segment Relocation parameter, and readback of the AUXMM (Auxiliary-Segment Memory Management) register, containing the relocation (XR<17:6>) and protection-mask (XM<15:12>) parameters for the auxiliary display-file segment. The register format is shown in Figure 3-9. This register functions identically to that of Select Code 4, with the exception that it applies to the Auxiliary rather than the Main segment. [The auxiliary segment can be used for display subroutines, Bit Map data and DMA Pixel Readback data.]

The memory-management parameters are cleared by Initialize.

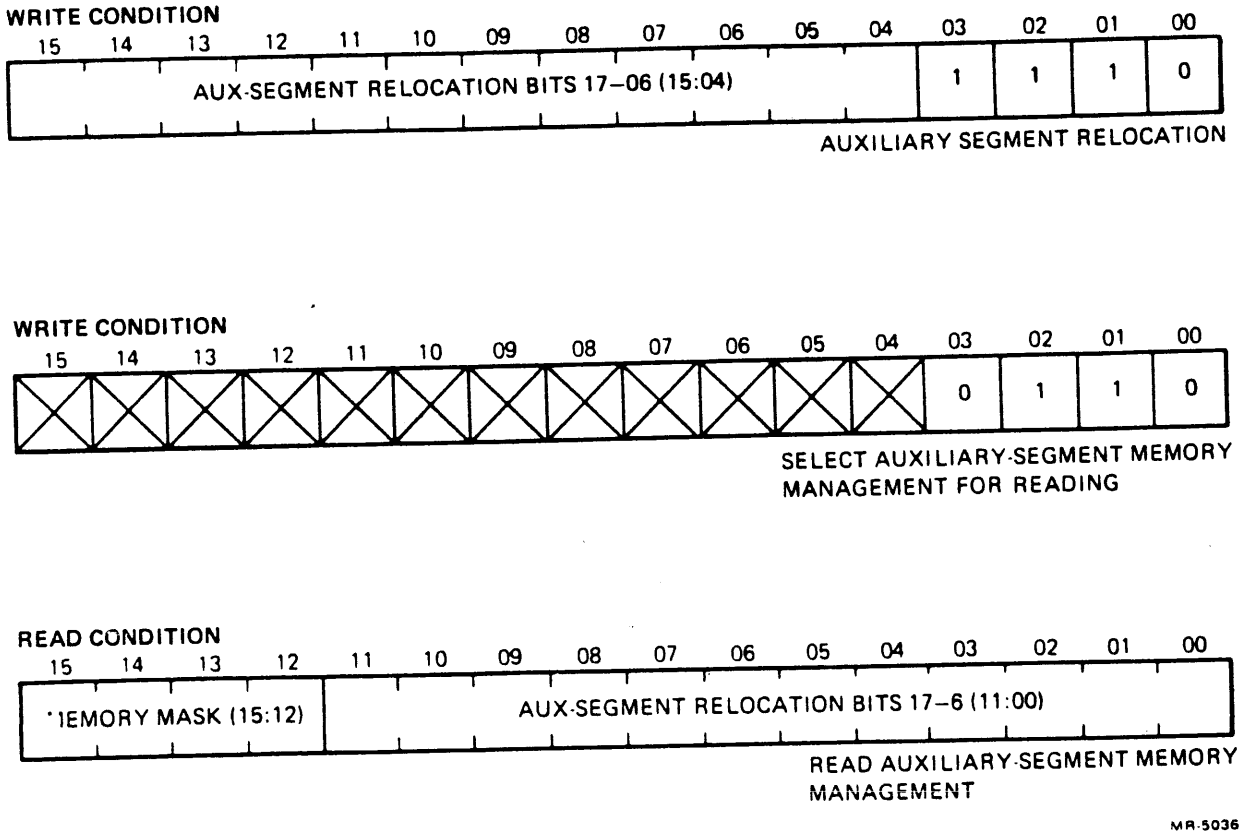


Figure 3-9
DSR Auxiliary-Segment/Relocation Register Format

3.3.2.8 Auxiliary-Segment Protection Mask/CBASE [Select=7] –

Selecting register 7 in the DSR bus location allows the 4-bit Auxiliary-Segment Protection Mask and Write-Protect bit to be written, and the CBASE (Character Base) Register to be read. Figure 3-10 shows the register format. This register functions similarly to that of Select Code 5, with the exceptions that it writes the Auxiliary (rather than Main) Protection Mask and Write-Protect, and reads back CBASE (rather than HBASE). The Auxiliary Segment write-protect appears in bit 14 of HBASE.

The CBASE register holds the data word loaded by the SET CHARACTER BASE display instruction: bit 0 specifies the segment containing the character routines (0 = Main, 1 = Auxiliary), and bits 1-15 specify the virtual starting address of the character dispatch area within the selected segment.

The CHARACTER BASE register is cleared by Initialize.

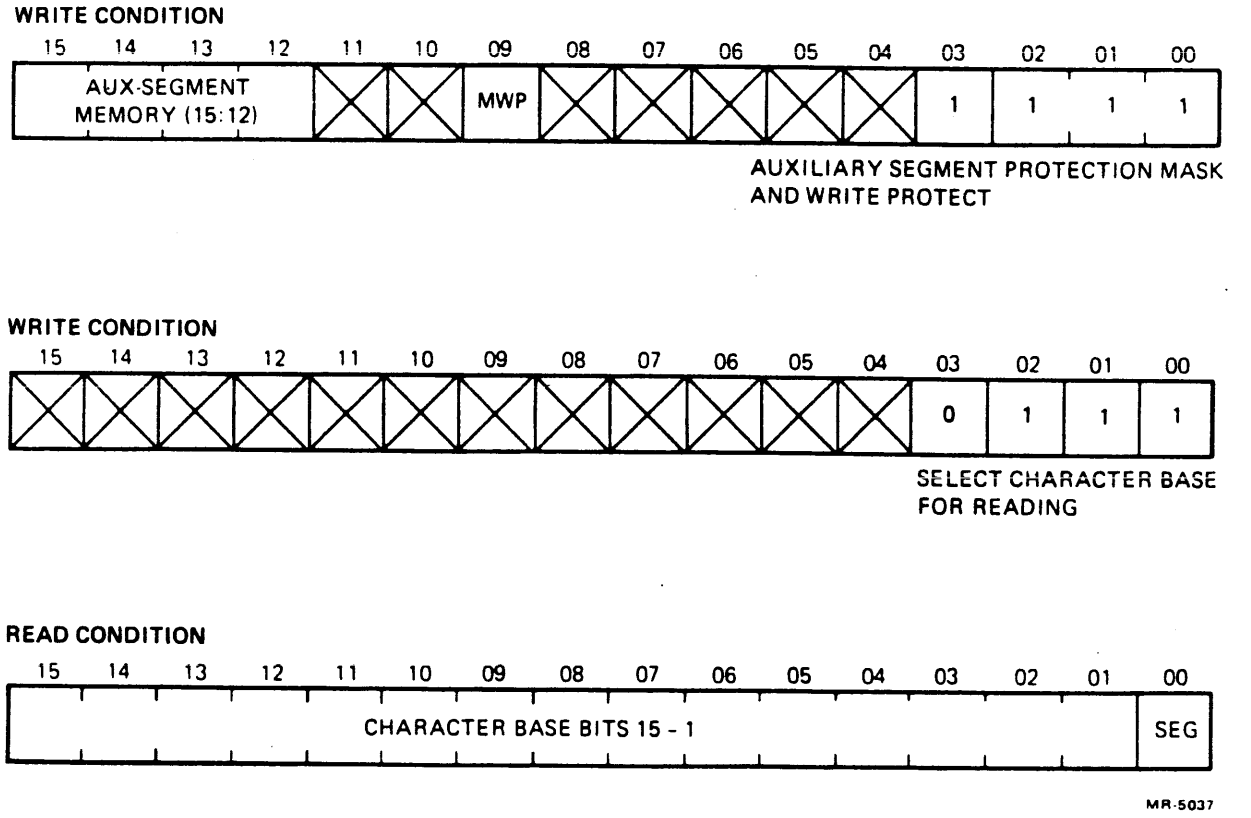


Figure 3-10
DSR Auxiliary-Segment/CBASE Register Format

3.3.3 X-Status Register (DXR) 7xxxx4

Reading the DXR location (general address 7xxxx4) presents the contents of the internal XSR register, which can contain either the current X-coordinate of the graphics position pointer (bits 0-10 of the internal XPOS register shifted left 1 place), the X-coordinate of a Joystick Match interrupt, or the X-coordinate of the cursor position on the currently-selected Joystick channel. Bit 15 is a flag indicating the type of data contained in DXR (0 = Graphics or Match position, 1 = Cursor).

Writing into the DXR location causes actions dependent upon the data written into bits 14 and 15 (Pixel Readback, Joystick Status Register write and/or cursor readback, restoration of X-Y graphics position to XSR & YSR, or Cursor-X-position write).

Figure 3-11 depicts the DXR register format under various conditions. Table 3-9 describes the actions obtained when writing into DXR.

NOTE

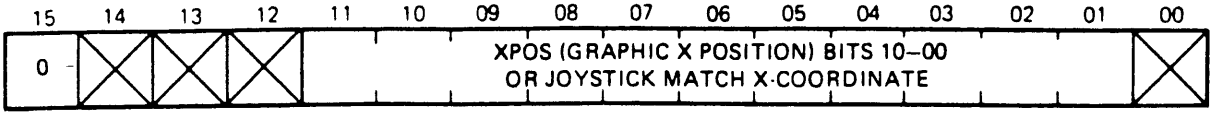
Any write into DXR causes the Display Processor to become momentarily "BUSY", so the program must wait for the STOP bit in DS: to set before attempting further accesses.

After the cursor status is read into DXR (Bit 15=1), bits 11-12 contain status for the selected joystick channel as follows:

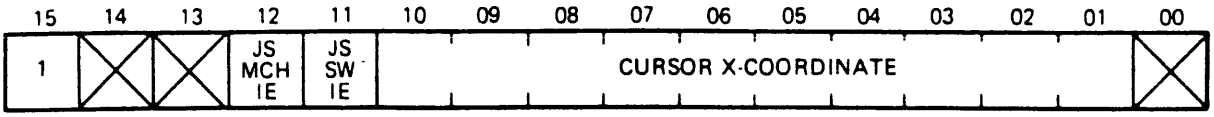
Bit 11: Indicates the state of the JOYSTICK SWITCH Interrupt Enable

Bit 12: Indicates the state of the CURSOR MATCH Interrupt Enable

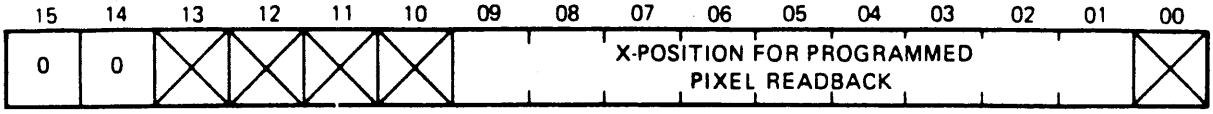
READ GRAPHICS



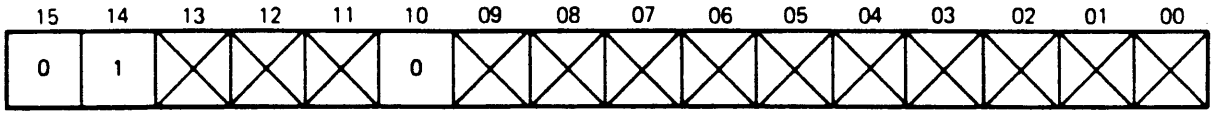
READ CURSOR



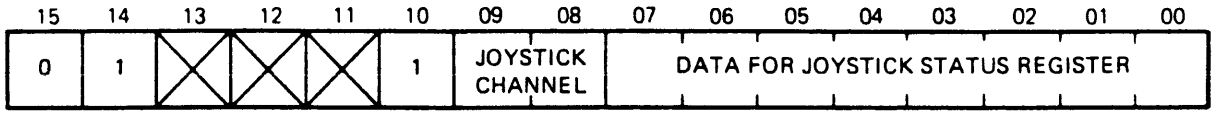
WRITE PERFORM PIXEL READBACK



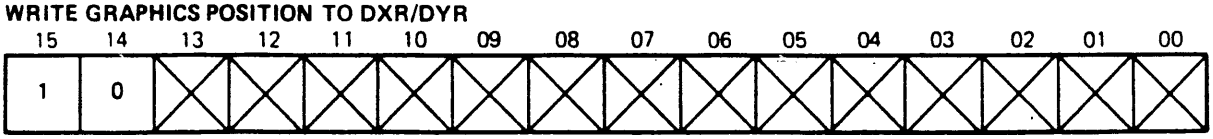
WRITE JS INTERRUPT CURSOR POSITION INTO DXR/DYR



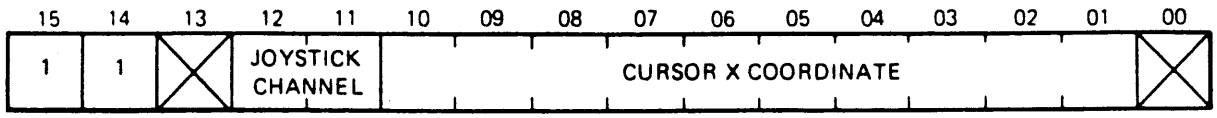
WRITE JS STATUS REGISTER



WRITE GRAPHICS POSITION TO DXR/DYR



WRITE CURSOR X COORDINATE



MR-5038

Figure 3-11
DXR Register Formats

Table 3-9
DXR Write Functions

Bit 15	Bit 14	Action
0	0	PIXEL READBACK: The following sequence is initiated: (1) Bits 11-0 of the data are written into XSR; the data is shifted right 1 place and loaded into the internal XPOS register. Processor becomes "busy". (2) A READ of Image Memory is performed at the coordinates specified in the XPOS & YPOS (Y-position) registers. Any memory channel in write-only or read/write mode responds. (3) Bits 9-0 of the data returned from memory are loaded into bits 9-0 of the DSR register: the remainder of DSR (bits 10-15) is preserved. (4) The internal DSR Register Select Code is cleared to 0, selecting the "real" DSR; the DPU returns to "idle" allowing registers to be read.
0	1	JOYSTICK STATUS: Action depends upon contents of bit 10. Bit 10 = 0: Reading of the cursor coordinates on the currently-selected Joystick channel is initiated (Display Processor becomes "busy"). DSR Register- Select code is cleared, selecting DSR (so STOP bit can be monitored). Cursor coordinates are returned in DXR and DYR, and the Display Processor returns to "idle". (Coordinates are returned only if a Joystick switch interrupt is present in the current channel. If no interrupt has been taken, the DATA READY Timeout error code will be loaded into the CSR). Bit 10 = 1: Bits 0-7 of the data is written to the Joystick Status Register (See Paragraph 3.5.2.1 for a description of the register). In addition, if Bit 6=1, the cursor coordinates on the selected channel (bits 8, 9) are read into XSR & YSR; the Display Processor is "busy" for the duration of the read.

Table 3-9 (cont'd)
DXR Write Functions

Bit 15	Bit 14	Action
1	0	RESTORE GRAPHICS POSITION: Loads the current contents of the internal XPOS and YPOS registers into XSR and YSR (for display in DXR & DYR).
1	1	WRITE CURSOR X-COORDINATE: Loads bits 1-10 of the data into the X cursor position of the channel selected by bits 11-12.

3.3.4 Y-Status Register (DYR) 7xxxx6

Reading the DYR location (general address 7xxxx6) presents the contents of the internal YSR register, which can contain either the current Y-coordinate of the graphics position pointer (bits 0-10 of the internal YPOS register shifted left 1 place), the Y-coordinate of a Joystick Match interrupt, or the Y-coordinate of the cursor position on the currently selected Joystick channel. Bit 15 is a flag indicating the type of data contained in DYR (0 = Graphics or Match position, 1 = Cursor). Reading functions identically to reading DXR except that Y information is presented.

Writing into the DYR location causes actions dependent upon the data written into bits 13, 14 and 15 (Pixel Readback, Memory Status Register write, "soft" Initialize, write Cursor Y Coordinate, or write Extended Cursor Control).

Figure 3-12 depicts the DYR register format under various conditions. Table 3-10 describes the actions performed when writing into DYR.

NOTE

Any write into DYR causes the Display Processor to become "BUSY", so the program must wait for the STOP bit in DSR to set before attempting further accesses. The DSR register-select code is cleared when DYR is written to facilitate the monitoring of STOP.

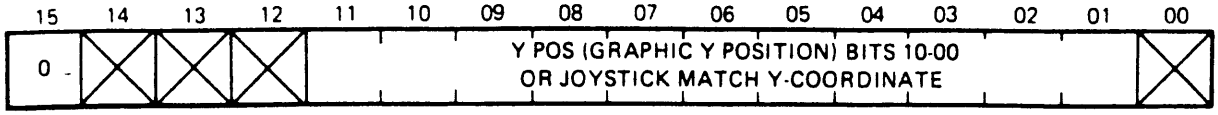
After the cursor status is read into YSR (Bit 15=1), bits 11-13 contain status as follows:

Bit 11: (SYNC INTL) "0" indicates the sync module is in "Non-Interlaced" mode.
"1" indicates the sync module is in "Interlaced" mode.

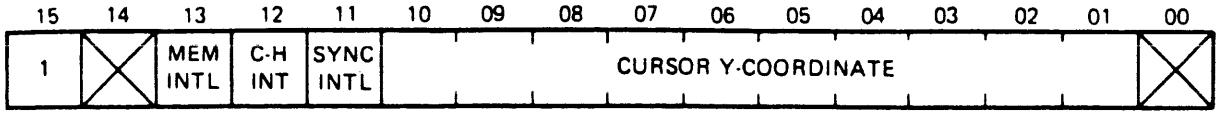
Bit 12: (C-H INT) Indicates the state of the Crosshair Intensity Enable.

Bit 13: (MEM INTL) "0" indicates the image memories are in "Non-Interlaced" mode.
"1" indicates the image memories are in "Interlaced" mode.

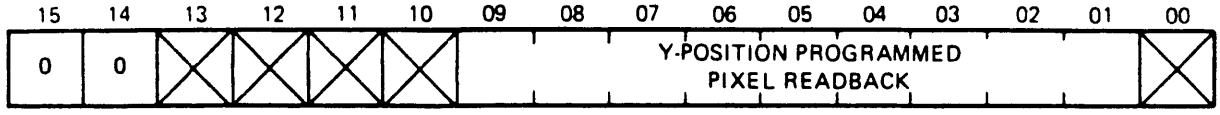
READ GRAPHICS



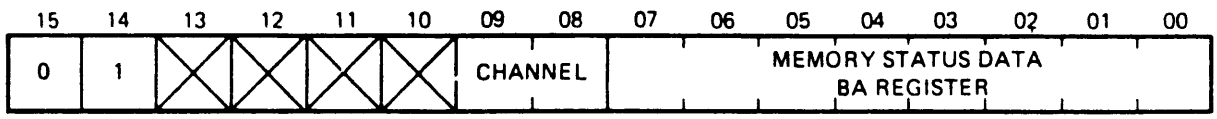
READ CURSOR



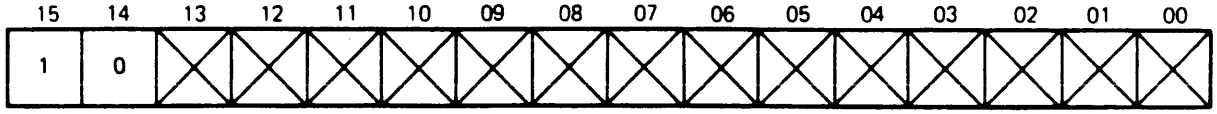
WRITE PERFORM PIXEL READBACK



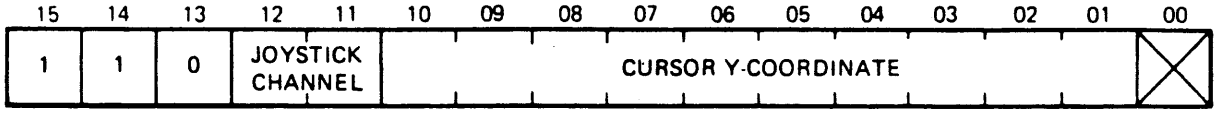
WRITE MEMORY STATUS



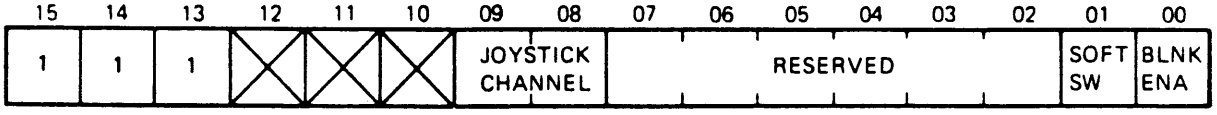
WRITE INITIALIZE



WRITE CURSOR Y-COORDINATE



WRITE EXTENDED CURSOR CONTROL



MR-5039

Figure 3-12
DYR Register Formats

Table 3-10
DYR Write Functions

Bit 15	Bit 14		Action
0	0	PIXEL READBACK:	The following sequence is initiated: (1) Bits 9-1 of the data written is shifted right 1 place and loaded into the internal YPOS register. The DPU becomes "busy". (2) A read of image memory is performed at the coordinates specified in the XPOS and YPOS registers. Any memory in Write-only or Read/Write mode responds. (3) Bits 9-0 of the data returned from memory are loaded into bits 9-0 of the DSR register (not all bits are necessarily valid). Bits 15-10 of DSR are preserved. (4) The internal DSR Register-Select code is cleared to 0, selecting the DSR. The DPU returns to "idle", allowing registers to again be accessed.
0	1	WRITE MEMORY STATUS BA:	Bits 0-7 of the written data are sent to the Image Memory STATUS BA register; bits 8 and 9 select the specific memory channel written. See the description of the STATUS C display instruction (Paragraph 3.5.2.11) for a description of the register function bits.
1	0	INITIALIZE	The DPU startup sequence is performed, initializing internal registers and performing a "self-test". DPC and the graphic position registers are cleared, PCSAVE is set to "empty" status, pending interrupts and flags are cleared, memory management registers are cleared, and CSR is cleared. If an error is detected during self-test, the error code will appear in the CSR. If all tests are passed, all image memories are placed in Write-only mode and cleared, and all Joystick channels are cleared.

Table 3-10 (cont'd)
DYR Write Functions

Bit 15	Bit 14		Action
1	1	w/Bit 13=0:	WRITE CURSOR Y-COORDINATE: Loads bits 1-10 of the data into the Y cursor position of the Joystick channel selected by bits 11-12. If the channel does not exist, a DATA READY TIMEOUT error will be indicated in the CSR.
1	1	w/Bit 13=1:	WRITE EXTENDED CURSOR CONTROL REGISTER: Loads bits 0 (Blink Enable) and 1 (Simulate Switch) into the Joystick channel selected by bits 8 and 9. Setting the Blink Enable causes any pixel with bit 8 set (=1) in the Image Memory feeding the SYNC (Joystick) channel to "blink" off and on while being displayed on the monitor. The cursor itself does not blink. Setting the Simulate Switch bit simulates closure of the manual joystick switch.

3.4 INTERRUPTS

The VSV11 is assigned a block of four interrupt vectors (eight 16-bit words). The beginning of the block is switch-selectable in the range 0 through 3760 (octal): the block must start on an even 16-byte boundary. Vectors within the block are allocated as shown in Table 3-11.

Table 3-11
Interrupt Vectors

Interrupt Condition	Offset within Block (Byte)	Factory Standard Address
STOP	0	320
CURSOR (J.S.) MATCH	+4	324
ERROR	+10	330
JOYSTICK SWITCH	+14	334

An interrupt condition arising during display processing causes processing to stop (processor returns to "idle"), either immediately or at the logical conclusion of the current display instruction. The JOYSTICK SWITCH interrupt can be initiated when the Display Processor is either busy or idle, while the others arise only while the processor is busy (they are mutually exclusive).

The interrupts are organized into two groups, A and B. Group A consists of the STOP and CURSOR MATCH interrupts. Group B consists of the ERROR and JOYSTICK SWITCH interrupts. The actual interrupt occurring as the result of a stop condition can be enabled/disabled via the STATUS A display instruction (Paragraph 3.5.2.10). When the stop interrupt is disabled, the conditions cause display processing to stop but no interrupt to be requested (unless the Force Stop Interrupt bit in CSR is set; Paragraph 3.3.2.4). The CURSOR MATCH condition is itself enabled/disabled via the JOYSTICK STATUS display instruction (Paragraph 3.5.2.1).

Group B interrupts are always enabled. However, the JOYSTICK SWITCH condition can be enabled/disabled via the JOYSTICK STATUS display instruction.

The presence of pending interrupts can be monitored and cleared via the FLAGS register (Paragraph 3.3.2.3) when the Display Processor is idle. The register will indicate a pending interrupt only when the PDP-11 CPU is running at or above the request level of the VSV11 itself (if the CPU were running below the VSV11's level, the interrupt would occur and the "pending" status cleared).

3.4.1 STOP Interrupt

The STOP interrupt is generated when the VSV11/VS11 system completes a LOAD STATUS A instruction, provided the Stop Interrupt Enable and Stop Interrupt bits are set and the VSV11/VS11 does a display stop. This interrupt is conditioned by bits 8, 9 and 10 of the LOAD STATUS A control instruction (Paragraph 3.5.2.10). These bits must be set to the one state in the display file to produce the STOP interrupt. If a previous STATUS A instruction has enabled the interrupt but did not stop (bit 10=0, bits 8 & 9 =1), or if the FORCE STOP INTERRUPT bit in CSR is set, a stop caused by writing into one of the VSV11 device registers will generate a STOP interrupt.

3.4.2 CURSOR MATCH Interrupt

CURSOR MATCH is an interrupt which can be manually initiated from the VSV11/VS11 joystick. This interrupt can be enabled by setting bits 2 and 3 of the JOYSTICK STATUS register, either by a control instruction (Paragraph 3.5.2.1) or a write into DXR from the host computer (Paragraph 3.3.3). The cursor video (bit 5 of the joystick status control instruction) should be set (one state) to allow positioning of the system monitor crosshairs with the joystick. When the position of the crosshairs matches a pixel position, and the joystick switch is pressed, the JOYSTICK MATCH interrupt is generated provided the Display Processor is writing to that Image Memory pixel position.

At the time the match between cursor coordinates and current graphic position (i.e., the display "writing" position) occurs, the Display Processor stops executing the display file, leaving the current coordinate (of the match position) in DXR and DYR for the program to read. The internal graphic position is, however, updated to the logical endpoint of the element (vector, histogram, etc.) being drawn, so that a Resume can continue the picture.

In typical use, an applications program will execute the display file once to draw the desired picture onto the screen, enable the joytick switch-interrupt (Paragraph 3.4.4), and then stop. When the user positions the cursor and depresses the switch, the program will be notified (via a Joystick Switch interrupt). The program will then start the display file again, but with the CURSOR MATCH interrupt enabled, to find the graphic element intersecting the cursor crosshairs.

3.4.3 ERROR Interrupt

The ERROR interrupt is produced whenever the Display Processor is executing a display file and one of the error conditions listed in Table 3-6 is detected. The ERROR interrupt is automatic (it cannot be disabled).

NOTE

Errors arising from programmed I/O operations (writing into DXR or DYR) cause the error code in CSR to be loaded, but no interrupt is generated.

3.4.4 JOYSTICK SWITCH Interrupt

JOYSTICK SWITCH is a manual interrupt which can be initiated from the VSV11/VS11 joystick control. This interrupt is conditioned (enabled/disabled) by bits 0 and 1 of the joystick status register in the VSV11/VS11 SYNC modules. This register may be loaded by the JOYSTICK STATUS control instruction, or by writing into the DXR register with bits 0 & 1 both written to 1, the JOYSTICK SWITCH interrupt is enabled on the selected channel; it is automatically disabled on all other channels.

With the interrupt enabled, action taken when the manual joystick switch is pressed depends upon the state of the Display Processor. If the DPU is executing the display file, it stops at the end of the current display instruction, loads the cursor coordinates into DXR and DYR (setting bit 15 of both registers) and generates the interrupt to the CPU). If the DPU is idle (not executing the display file) when the switch is pressed, only the interrupt is generated; the program in the CPU must cause the cursor coordinates to be retrieved into DXR and DYR by writing 40000 (octal) into DXR.

3.5 VSV11/VS11 INSTRUCTION SET

The VSV11/VS11 instruction set consists of over 30 instructions, organized into four basic types:

1. Graphic-Mode instructions, including Vector, Point, Character, Graph/Histogram and Run-Length. The Graphic-Mode instructions set the basic operating characteristic of the Display Processor, determining the interpretation of the Graphic Data instructions which follow.

2. Graphic Data instructions, with various formats depending upon the current Graphic Mode. These instructions define coordinates and graphic entities to be shown on the system monitor (CRT).

3. Control instructions, providing for setup of Image Memory and joystick channels, branching of the display program within the display file (Jump and Jump-to-Subroutine, and subroutine return), clearing of image memories and No-Op.

4. Special Graphic instructions, including Bit-Map (pixel-by-pixel writing into Image Memory) and DMA Pixel Readback (from Image Memory into PDP-11 memory).

Figure 3-13 is a summary which shows the VSV11/VS11 instruction set word formats, including the formats of data words accompanying the basic instructions. Except where specifically indicated, all unused bits in the instructions should be set to zero when the display file is programmed. Following this rule will ensure that current display programs will be compatible with future versions of the VSV11/VS11 with expanded instruction sets.

Display file words having bit 15 set (1) are termed "control" or "instruction" words and are normally interpreted as Graphic-Mode, Control, or Special instructions.

In such case, bits 14-11 define a basic instruction Op-Code. Interpretation of bits 10-0 depends upon the basic Op-Code: for the Graphic Mode Op-Codes these bits define pixel data (intensity/color), while for the Control and Special Op-Codes they provide further definition of the operation to be performed or data to be loaded into various registers.

Graphic Data instruction words are those in which bit 15 is clear (0). These words are interpreted within the context of the current Graphic-Mode.

Table 3-12 summarizes the octal word configuration of the basic Graphic-Mode, Control and Special instructions, serving as a brief programmer's reference.

The following paragraphs describe each of the VSV11/VS11 instructions in detail.

NOTE

Unused/undefined instruction Op-Codes function as a No-Op if the EN RCHK bit in CSR is 0. They cause a stop with ERROR interrupt if EN RCHK is 1.

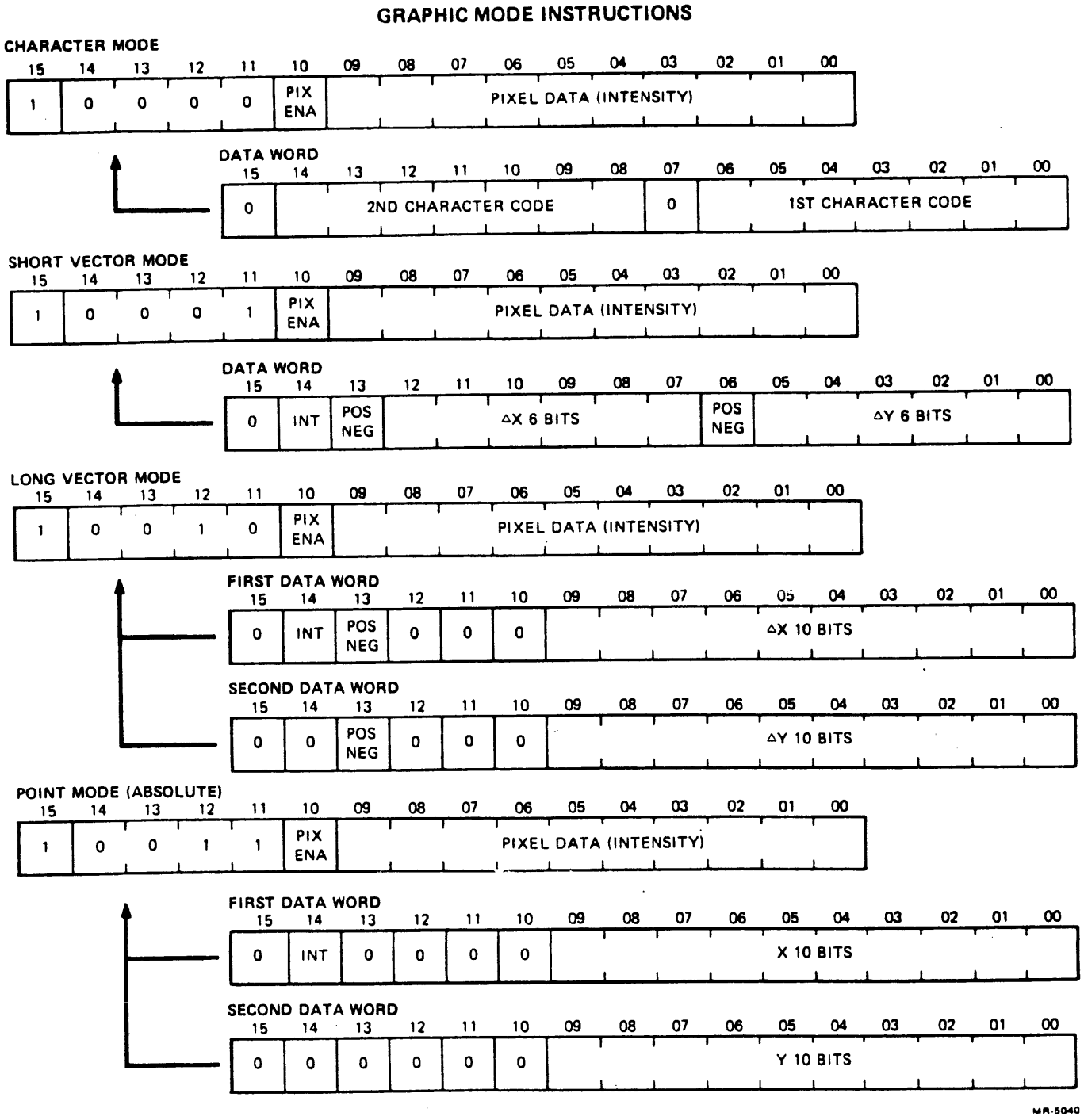


Figure 3-13
VSV11/VS11 Instruction Word Summary
(sheet 1 of 5)

GRAPHIC MODE INSTRUCTIONS (CONT)

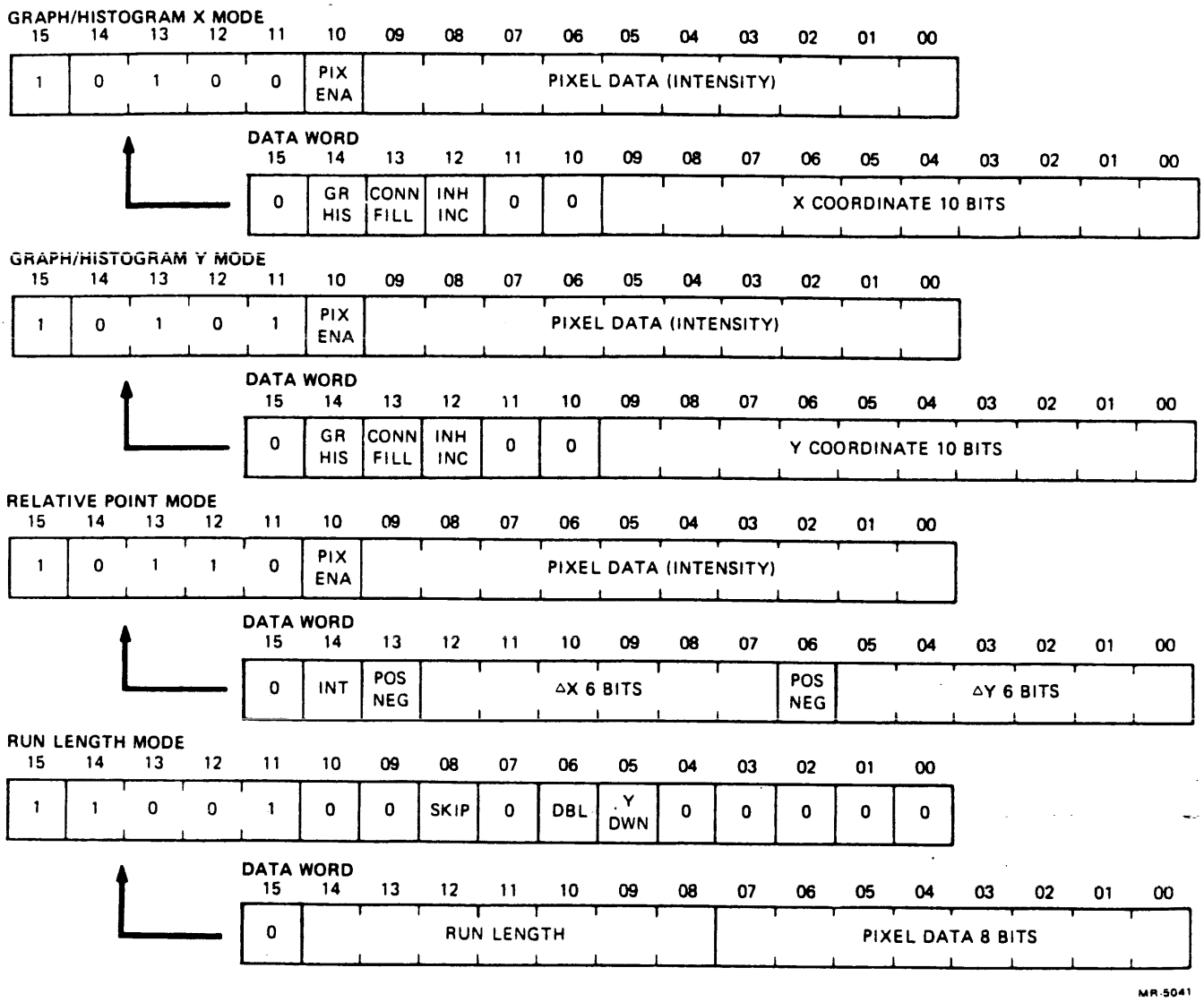


Figure 3-13
VSV11/VS11 Instruction Word Summary
(sheet 2 of 5)

CONTROL MODE INSTRUCTIONS

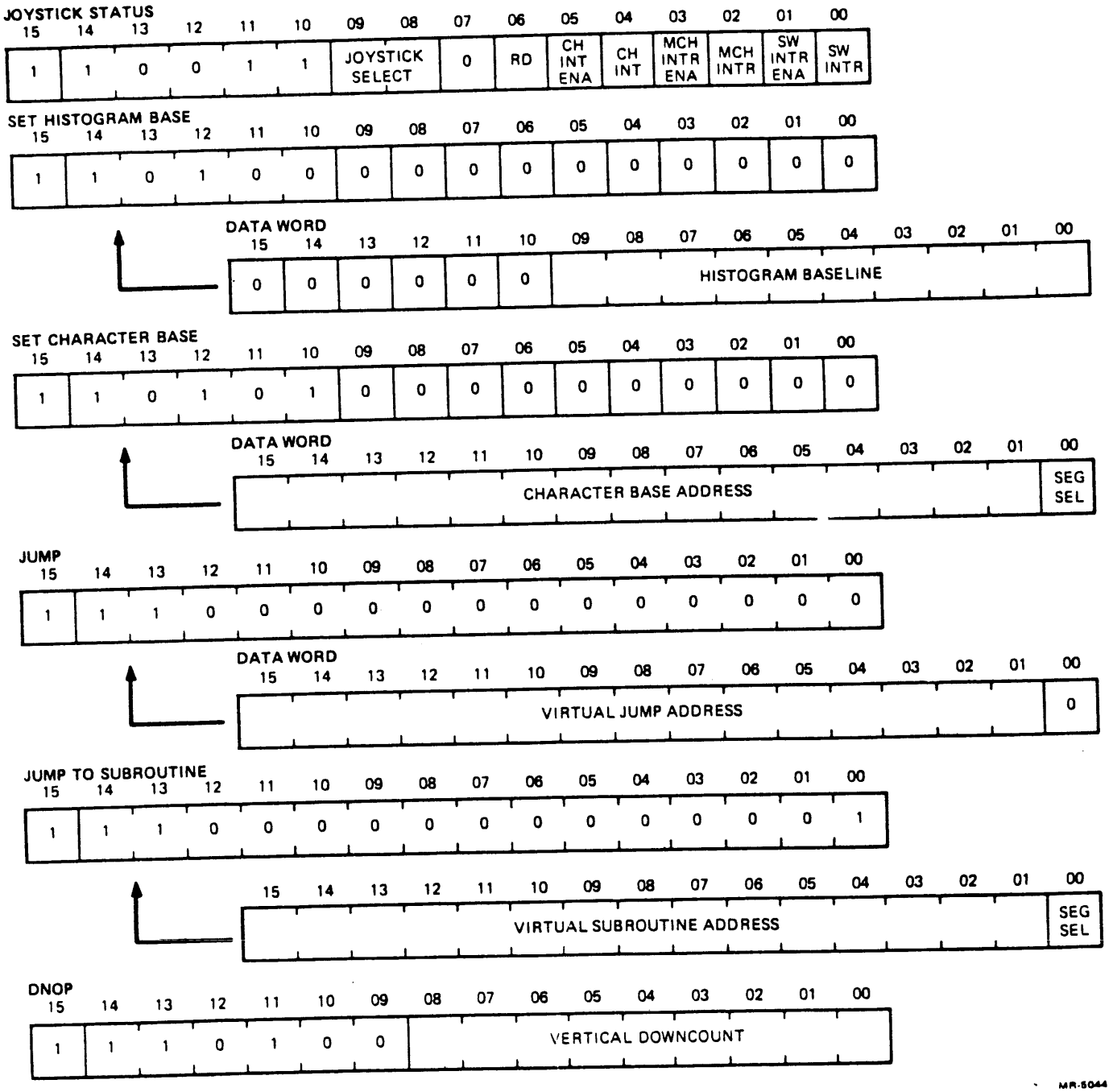


Figure 3-13
VSV11/VS11 Instruction Word Summary
(sheet 3 of 5)

CONTROL MODE INSTRUCTIONS (CONT)

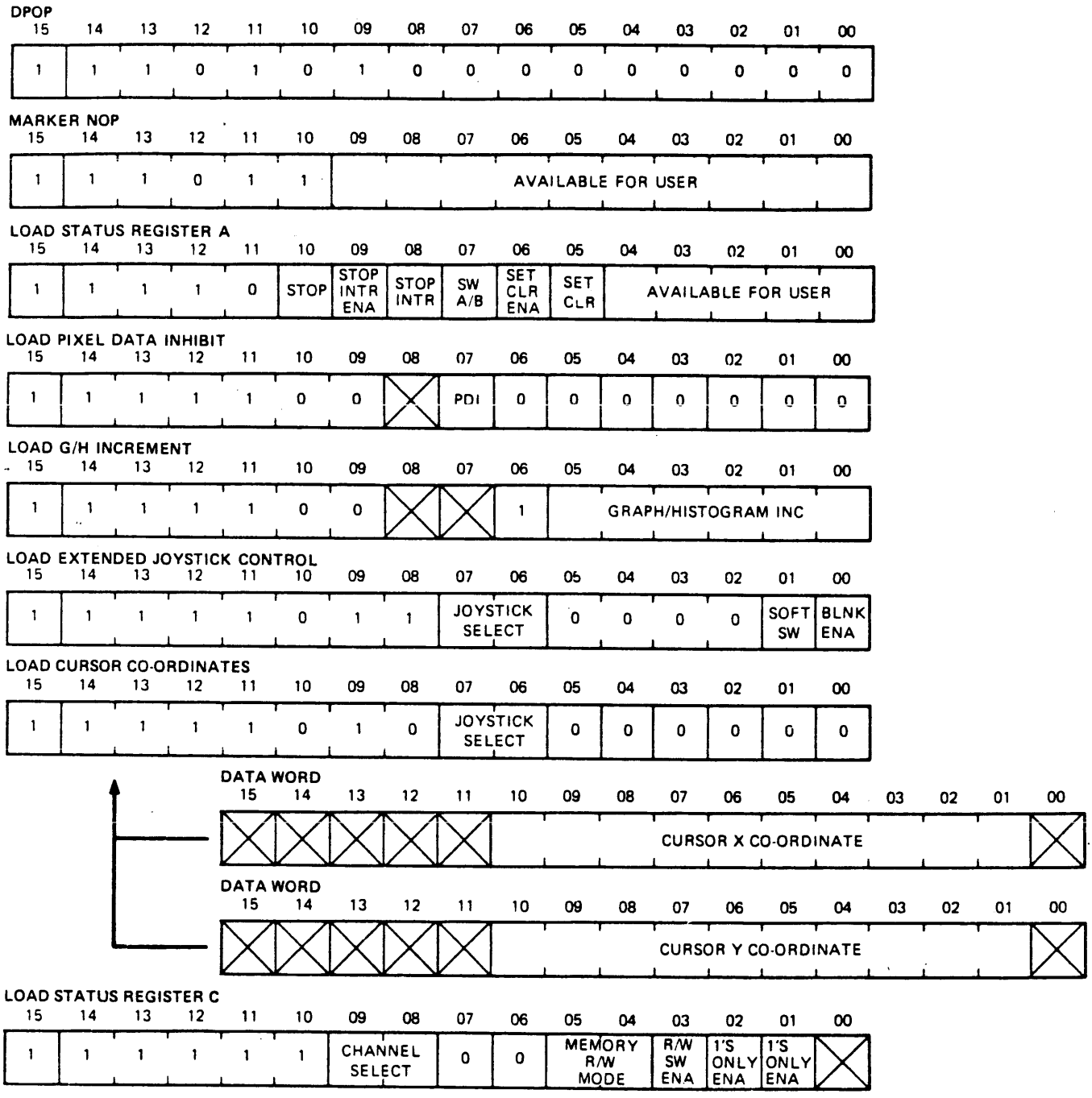
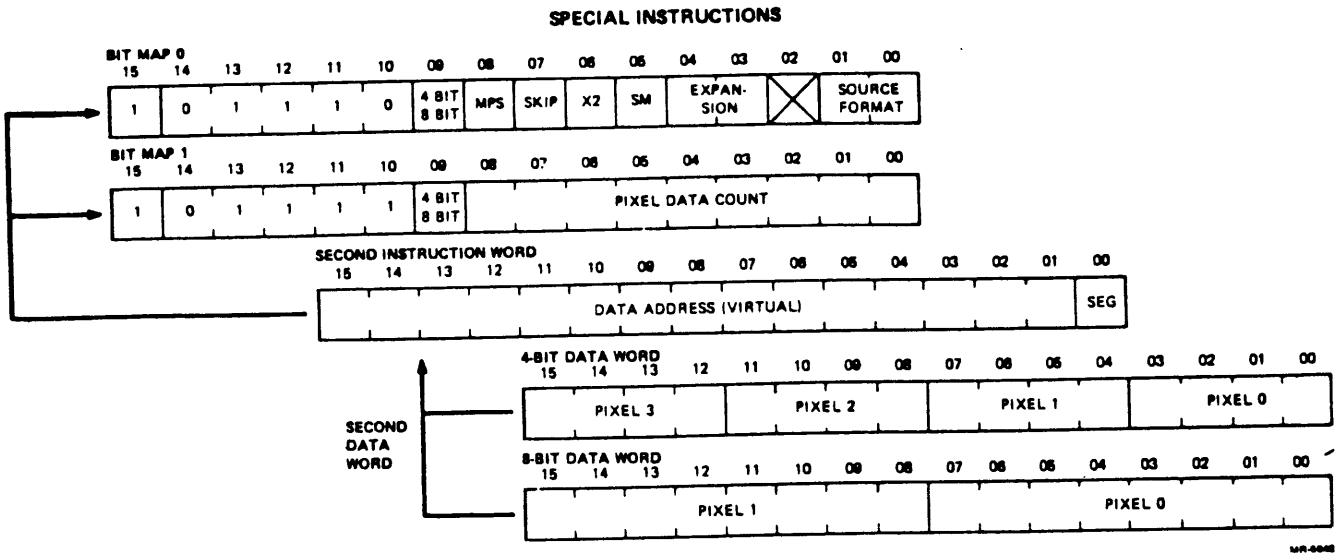


Figure 3-13
VSV11/VSI1 Instruction Word Summary
(sheet 4 of 5)



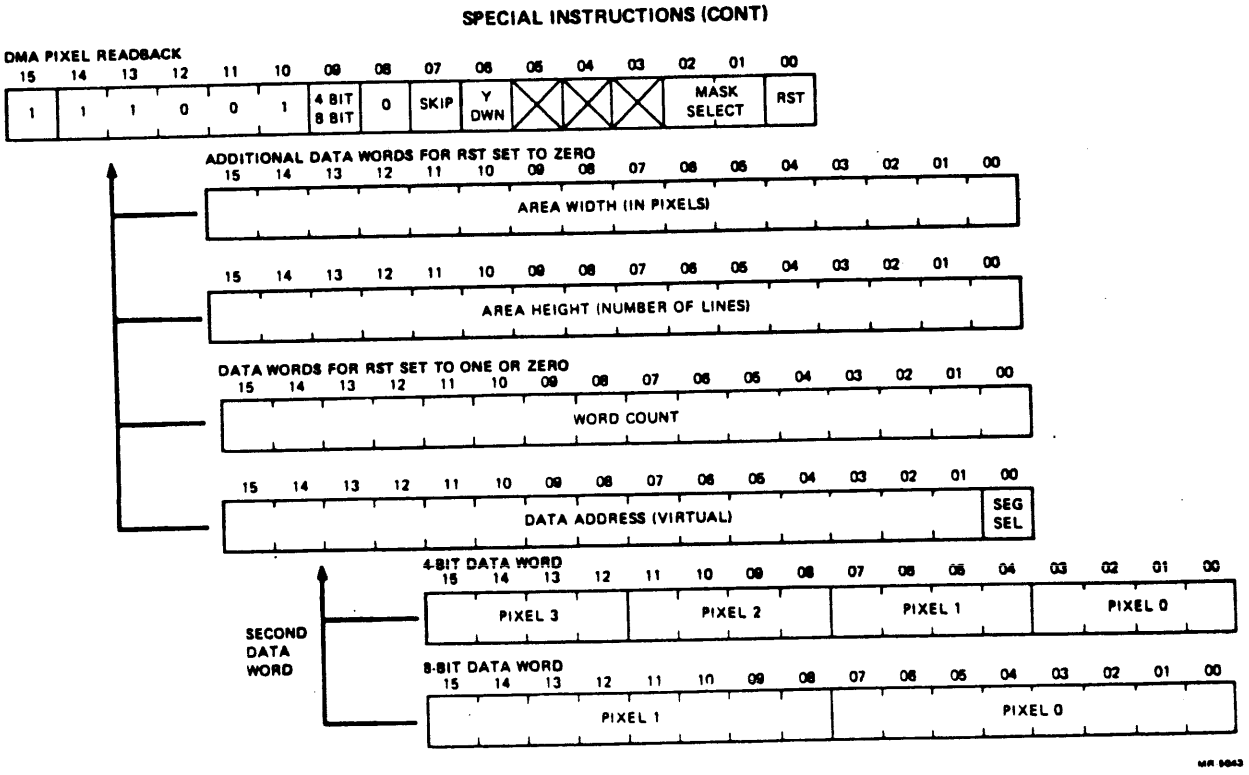


Figure 3-13
VSV11/VS11 Instruction Word Summary
(sheet 5 of 5)

Table 3-12
VSV11/VS11 Instruction Set Summary

I-Bits 14-10	Instruction	Octal Codes
00000 00001	Set CHARACTER Mode [& Load Pixel Data]	100000 102000 - 103774
00010 00011	Set SHORT VECTOR Mode [& Load Pixel Data]	104000 106000 - 107774
00100 00101	Set LONG VECTOR Mode [& Load Pixel Data]	110000 112000 - 113774
00110 00111	Set ABSOLUTE POINT Mode [& Load Pixel Data]	114000 116000 - 117774
01000 01001	Set GRAPH/HISTOGRAM-X Mode [& Load Pixel Data]	120000 122000 - 123774
01010 01011	Set GRAPH/HISTOGRAM-Y Mode [& Load Pixel Data]	124000 126000 - 127774
01100 01101	Set RELATIVE POINT Mode [& Load Pixel Data]	130000 132000 - 133774
01110	BIT-MAP-0 (4-Bit Pixel Data) BIT-MAP-0 (8-Bit Pixel Data)	134000 [+400 for 8-bit Memory] 135000 [+200 for Skip] [+100 for Double Expand] [+40 for Smoothing] [+0, 10, or 20 for x1, x2, or x4 Expansion] [+0 for 32x32 Array, +1 for 64x64 Array, +2 for 128x128 Array, or +4 for 256x256 Array]
01111	BIT-MAP-1 (4-bit Pixel Data) BIT-MAP-1 (8-bit Pixel Data)	136000 + Count [000-777] 137000 + Count [000-777]
10000 10001	(Reserved) (Reserved)	140000 - 141777 142000 - 143777
10010	Set RUN-LENGTH Mode	144000 [+400 for Line-Skip] [+100 for Double-Count] [+40 for Step Y Down]
10011	JOYSTICK STATUS (Channel 0) (Channel 1) (Channel 2) (Channel 3)	146000 [+100 to Read Cursor] 146400 [+60 to Enable Crosshairs 147000 +40 to Disable Crosshairs] 147400 [+14 to Enable Match Int., +10 to Disable Match Int.] [+3 to Enable Switch Int., +2 to Disable Switch Int.]

Table 3-12 (cont'd)
VSV11/VS11 Instruction Set Summary

I-Bits 14-10	Instruction	Octal Code(s)
10100	SET HISTOGRAM BASE (Reserved)	150000 150001 - 151777
10101	SET CHARACTER BASE (Reserved)	152000 152001 - 153777
10110 10111	(Reserved) (Reserved)	154000 - 155777 156000 - 157777
11000	JUMP (DJUMP) JUMP-TO-SUBROUTINE (Reserved)	160000 160001 160002 - 161777
11001	DMA PIXEL READBACK (Start) (Restart)	162000 [+1000 for 8-Bit Data] 162001 [+200 for Line-Skip] [+100 for Step Y Down] [+0 for 2-bit Mask, +2 for 4-bit Mask, +4 for 6-bit Mask, or +6 for 8-bit Mask]
11010	Display NO-OP (DNOP) Display POP (Return)	164000 + Down-Co t [000-777] 165000
11011	MARKER NO-OP	166000 - 167777
11100 11101	LOAD STATUS A LOAD STATUS A & STOP	170000 [+1400 to Enable Stop Int. 172000 +1000 to Disable Stop Int.] [+200 to Switch Memory Mode] [+140 to Clear Image Memory, +100 to Set Image Memory]
11110	CLEAR PIXEL DATA INHIBIT SET PIXEL DATA INHIBIT LOAD GRAPH/HISTOGRAM INCREMENT LOAD CURSOR COORDINATES LOAD EXTENDED JOYSTICK CONTROL	174000 174200 174100 + [Increment 00-76] 175000 [+0, 100, 200 or 300 for Channel 0, 1, 2 or 3] 175400 [+0, 100, 200 or 300 for Channel 0, 1, 2 or 3] [+1 to Enable Blink] [+2 to Turn on Switch]
11111	LOAD STATUS C (Channel 0) (Channel 1) (Channel 2) (Channel 3)	176000 [+0 for PROTECT Mode, 176400 +20 for WRITE-Only Mode, 177000 +40 for READ-Only Mode, or 177400 +60 for READ/WRITE Mode] [+10 to Enable Switch] [+6 to Enable 1's-Only Mode, +4 to Disable 1's-Only Mode]

3.5.1 GRAPHIC MODE Instructions

The eight Set Graphic Mode instructions are:

CHARACTER
SHORT VECTOR
LONG VECTOR
ABSOLUTE POINT
GRAPH/HISTOGRAM X
GRAPH/HISTOGRAM Y
RELATIVE POINT
RUN-LENGTH

The VSV11/VS11 Display Processor is always considered to be "in" one of these modes, such that any Graphic-Data instruction (indicated by a display-file word having bit 15=0) encountered during processing is interpreted within the context of the current graphic mode.

A display file typically consists of a Graphic-mode-setting instruction followed by a string of graphic-data instructions. The string can be of any length (up to the end of the current virtual display file segment) and can contain embedded Control instructions.

Figure 3-14 illustrates the word format of the Set Graphic Mode instructions. Table 3-13 describes the function of each field. The following paragraphs provide a description of each instruction, along with its associated Graphic-Data instuction.

NOTE

The action of bit 10 of the instruction, PIXEL DATA ENABLE, can be inhibited by the SET PIXEL-DATA-CHANGE INHIBIT control instruction. Refer to Paragraph 3.5.2.13.

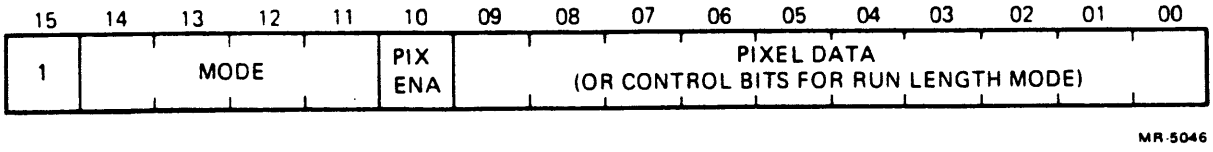


Figure 3-14
Set-Graphic-Mode Instruction Format

Table 3-13
Set-Graphic-Mode Instruction Field Assignments

Bit	Name	Description
15	-	1 indicates Control word
14-11	MODE	0000 = Character Mode 0001 = Short Vector Mode 0010 = Long Vector Mode 0011 = Absolute Point Mode 0100 = Graph/Histogram X Mode 0101 = Graph/Histogram Y Mode 0110 = Relative Point Mode 1001 = Run-Length Mode
10	PIXEL DATA CHANGE ENABLE (except Run-Length mode)	1 enables bits 9-0 into Pixel Data register (must be 0 for Run-Length mode)
9-0	PIXEL DATA (intensity or color) (except Run-Length mode)	For Monochrome System: Bit 9 = MSB, Bit 6 LSB Bits 5-0 for future expansion Bits 9-6 = 1111 = Maximum Inten. Bits 9-6 = 0000 = Zero Intensity For Basic Color System: Bits 9,8 = Green Bit 7 = Red Bit 6 = Blue Bits 5-0 for future expansion

3.5.1.1 CHARACTER Mode -

There are two instructions for this graphic mode. The first is a control instruction which sets the VSV/VS11 into Character mode (mode bits 14-11 = 0000) and is illustrated in Figure 3-14. Pixel data (bits 9-0) controls the intensity of the displayed pixel in a black and white system, or the color of the displayed pixel in a color system. Sixteen shades of gray or 16 colors can be specified in the 10 bits of pixel data. The pixel data is enabled by setting bit 10 to a one.

The Character Mode instruction is followed by one or more Character Data instructions (Figure 3-15 and Table 3-14). Two 7-bit character codes can be specified in the character data

instruction. The character codes can be 7-bit ASCII or some other code as defined by the user. The character codes are used to specify the index into a table of dispatch addresses, which in turn specify the starting addresses of display file subroutines in memory. The display file subroutine can be a routine to draw alpha-numerics or graphics on the system monitor. Since bit 7 is an unused bit, this bit must be set to zero. The SET CHARACTER BASE control instruction (Paragraph 3.5.2.2) is used in the character mode to specify the base (starting) address of the character dispatch table.

During operation in the Character mode, a byte (character) fetched from the display file is shifted left one place (to make a word index into the host CPU memory) and the result is added to the current contents of the CHARACTER BASE register. This sum specifies an address within the dispatch table, from which is fetched the starting address of the display subroutine responsible for drawing the character. Bit 0 of the CHARACTER BASE register specifies the segment in which the dispatch table and the display subroutine reside: bit 0=0 specifies the Main display file segment, while bit 0=1 specifies the Auxiliary segment. (The dispatch table and the display subroutine must always reside in the same segment).

Before execution of the display subroutine begins, the current contents of the Display Program Counter (DPC), which contains the address of the next Character Data instruction in the Main segment, is saved in an internal register (PCSAVE). A DPOP instruction (Paragraph 3.5.2.4) at the end of the display subroutine restores the DPC from PCSAVE to continue execution in character mode.

The following restrictions apply to Character mode:

1. A SET CHARACTER MODE instruction cannot occur within a display subroutine (including one called via the DJMS instruction).

2. A DJMS (Display-Jump-to-Subroutine), BIT-MAP, or DMA PIXEL READBACK instruction cannot occur within a display subroutine, since for each of these instructions the DPC must be saved in the PCSAVE register.

3. A Graphic Data instruction cannot occur in the display subroutine before occurrence of a Set Graphic mode instruction that takes the Display Processor out of Character mode.

Occurrence of any of the above restrictions results in a SEQUENCE ERROR stop and interrupt.

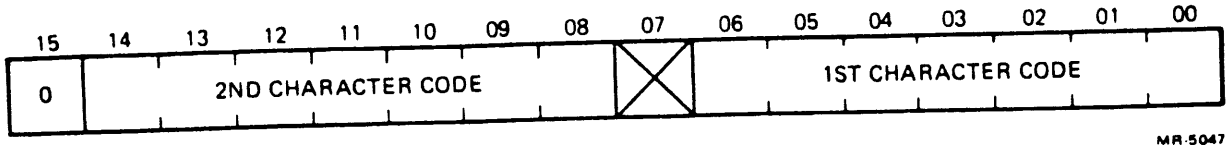


Figure 3-15
Character Data Word Format (Mode 0000)

Table 3-14
Character Data Word Field Assignments

Bit	Name	Description
15	-	0 indicates Data word
14-8	2nd Character Code	Character Code (could be 7-bit ASCII). This code is saved internally while the 1st character code of the word is being processed.
7	Reserved	Must be written to 0
6-0	1st Character Code	Character Code (could be 7-bit ASCII). After the data word is fetched, this field is the first character processed. It is shifted left 1 place and added to the contents of the CHARACTER BASE register to obtain an entry in the character dispatch table; this entry, in turn, contains the address of the character drawing routine to be executed.

3.5.1.2 SHORT VECTOR Mode -

A Graphic Mode instruction with a mode code of 0001 for bits 14-11 places the Display Processor into the Short Vector mode. Pixel data, controlling the intensity or color of the vectors to be subsequently displayed is specified in instruction bits 9-0 (if bit 10=1) (Figure 3-14).

Figure 3-16 shows the format of the Short Vector Data instructions which follow the Short Vector Mode instruction. Table 3-15 describes each field. Six bits each of the X and Y components of the vector are specified in the Short Vector Data Word, along with a sign bit for each component. The sign bits specify the direction for each component: a 0 in a sign position specifies a positive direction, while a 1 specifies a negative direction. Bit 14 of the data word (INTENSIFY) must be set to a one to cause the Image Memory to be written (i.e., to make the vector visible on the system monitor or overwrite a vector already existing in the Image Memory). The X and Y displacement parameters (magnitudes) are based upon a full screen resolution of 1024 points. In the VSV11/VS11, with a full-screen resolution of 512 points (pixels), the least significant bit of each Delta magnitude is not used and should be written as 0. If the LSB is nonzero, a RESERVED OPERATION error stop is taken if the EN RCHK bit in the CSR is one. If EN RCHK=0, the LSB is ignored and considered to be zero. The significant five bits of the delta components of a short vector can therefore specify a vector of up to 32 pixels in length (both the starting point and the endpoint of a vector are written if INTENSIFY = 1).

A vector is drawn beginning at the current graphic position, as held in the internal XPOS and YPOS registers and represented in XSR and YSR. Following execution of the vector data instruction, the current graphic position is updated to the final endpoint of the vector (i.e., XPOS $\pm$ Delta-X, YPOS $\pm$ Delta-Y). If the INTENSIFY bit, bit 14, in that data word is zero, only the graphic position is updated (actual writing of image memory is bypassed).

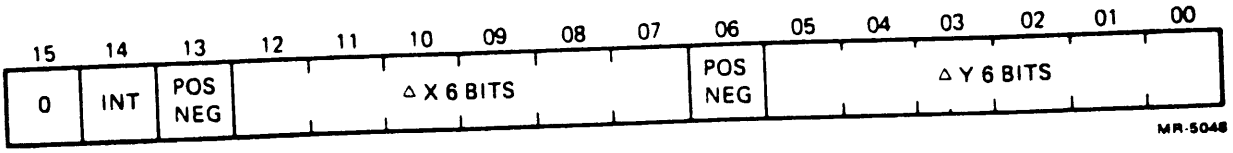


Figure 3-16
Short Vector Data Word Format (Mode 0001)

Table 3-15
Short-Vector Data Word Field Assignments

Bit	Name	Description
15	-	0 indicates Data word
14	INT (Intensify)	1 causes the vector to be written ("intensified"); 0 causes the graphic position to be updated to the logical endpoint, but no pixel data is written into image memory.
13	± X (Positive or Negative X)	0 specifies that the X component moves to the right (+); 1 specifies that the X component moves to the left (-).
12-7	DELTA-X	6-bit magnitude of the X (horizontal) component of the vector. (Note that the LSB is reserved).
6	± Y (Positive or Negative Y)	0 specifies that the Y component moves up (+) 1 specifies that the Y component moves down (-)
5-0	DELTA-Y	6-bit magnitude of the Y (vertical) component of the vector. (Note that the LSB is reserved).

3.5.1.3 LONG VECTOR Mode -

A minimum of three instructions are required for the Long Vector mode. The first instruction sets the Long Vector mode (Figure 3-14) by specifying a mode code of 0010 for bits 14-11. Pixel data is specified in bits 9-0. Bits 9-0 control the intensity of the displayed vector in a black and white system, or control the color of the vector in a color system. Sixteen shades of gray or 16 colors can be specified. Bit 10 must be set to a one to enable pixel data bits 9-0.

The Long Vector mode instruction is followed by at least two Long Vector Data instructions (Figure 3-17 and Table 3-16). The first Long Vector Data instruction specifies the 10-bit magnitude of the DELTA-X component of the vector and the sign of the DELTA-X component. Bit 14 of the first word must be set to cause the vector to be written into image memory (i.e., make the vector visible on the system monitor).

After the first data instruction has been processed, the VSV11/VS11 automatically fetches the second long vector data instruction. The second data instruction specifies the 10-bit magnitude of the DELTA-Y component of the vector and the sign of the DELTA-Y component. Unused bits in both data instructions (including bit 0 of the DELTA-X & DELTA-Y magnitudes must be written to zeros.

Operation of the long vector mode is similar to that of short vector mode, but, since the long vector mode has 10 bits of DELTA-X and DELTA-Y, the length of a vector can be greater than that of the short vector mode. However, since two data instructions must be fetched from the LSI-11 memory in long vector mode, two bus transactions are required. The display of multiple long vectors requires multiple pairs of the first and second long vector data instructions.

The nine significant bits of the DELTA-X and DELTA-Y magnitudes allow drawing of a vector of up to 512 pixels in length (both the starting point and the endpoint of the vector are drawn).

NOTE

The Delta-X and Delta-Y magnitudes are based on a full-screen resolution of 1024 points, to allow for system expansion. In the VSV11/VS11 system of 512-point resolution, the least significant bits of Delta-X and Delta-Y (bit 0 of the data words) are reserved and must be written to 0.

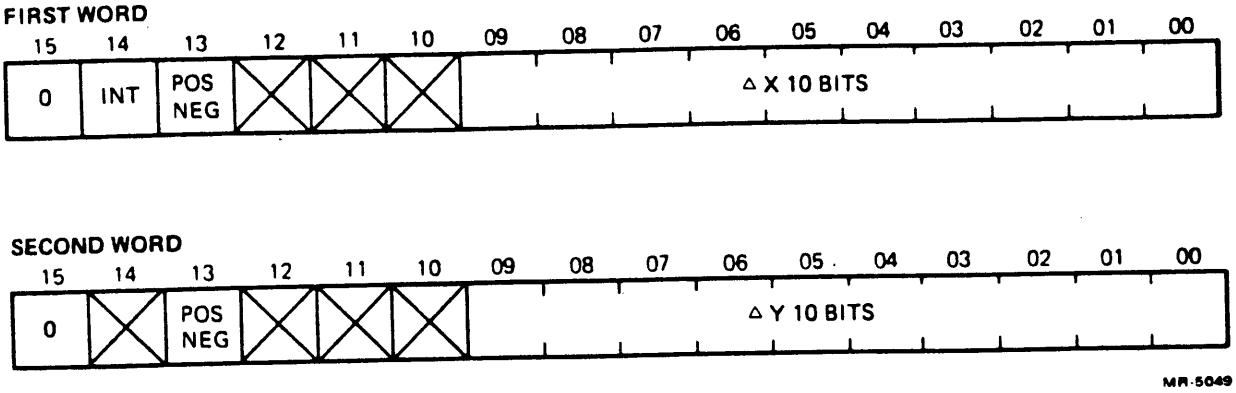


Figure 3-17
Long Vector Data Word Format (Mode 0010)

Table 3-16
Long Vector Data Word Definitions

	Bit	Name	Definition
1st word	15	-	0 indicates Data word
	14	INT (Intensify)	1 allows vector to be written 0 causes only the Graphic Position to be updated
	13	±X X Positive or Negative	0 specifies that the Delta-X component moves to the right (+) 1 specifies that the Delta-X component moves to the left (-)
	12-10	Reserved	Must be written to 0
	9-0	DELTA-X	10-bit magnitude of the X component of the vector. Bit 0 must be written to 0.
2nd word	15	-	0 indicates Data word
	14	Reserved	Must be written to 0
	13	±Y Y Positive or Negative	0 specifies that the Delta-Y component moves up (+) 1 specifies that the Delta-X component moves down (-)
	12-10	Reserved	Must be written to 0
	9-0	DELTA-Y	10-bit magnitude of the Y component of the vector. Bit 0 must be written to 0.

3.5.1.4 ABSOLUTE POINT Mode -

The Absolute Point mode is used to position the image or subimage at some absolute position on the system monitor screen. This differs from the short and long vector modes as these vector modes draw lines relative to the position of previously drawn operations (vector, points, etc.). In short and long vector modes a Delta-X and Delta-Y are specified with regards to the current display position. In the point mode, X and Y are specified as absolute coordinates. Point mode should always be used as one of the first graphic instructions transferred to the VSV11/VS11. This defines the starting point of a system monitor image.

A minimum of three instructions are required for the Absolute Point mode. The first instruction sets the point mode (Figure 3-14) by specifying a mode code of 0011 for bits 14-11. Pixel data (intensity level for black and white system, or pixel color for color systems) is specified in bits 9-0. Sixteen shades of gray or 16 colors can be specified with bits 9-0. Bit 10 must be set to a one to enable pixel data bits 9-0.

The Absolute Point mode instruction is followed by at least two Absolute Point data instructions (Figure 3-18 and Table 3-17). The first point data instruction specifies an absolute X-position, while the second point data instruction specifies an absolute Y-position. Bit 14 of the first point data instruction must be set to a one to write the point into Image Memory (make the point visible on the system monitor screen or erase a previously written point). Unused bits in both instructions must be written to zeros. A display file could consist of a series of Point Data instructions to position a number of points at various locations on the system monitor. This requires first and second point data instruction pairs for each beam position. Only one Absolute Point mode instruction is required.

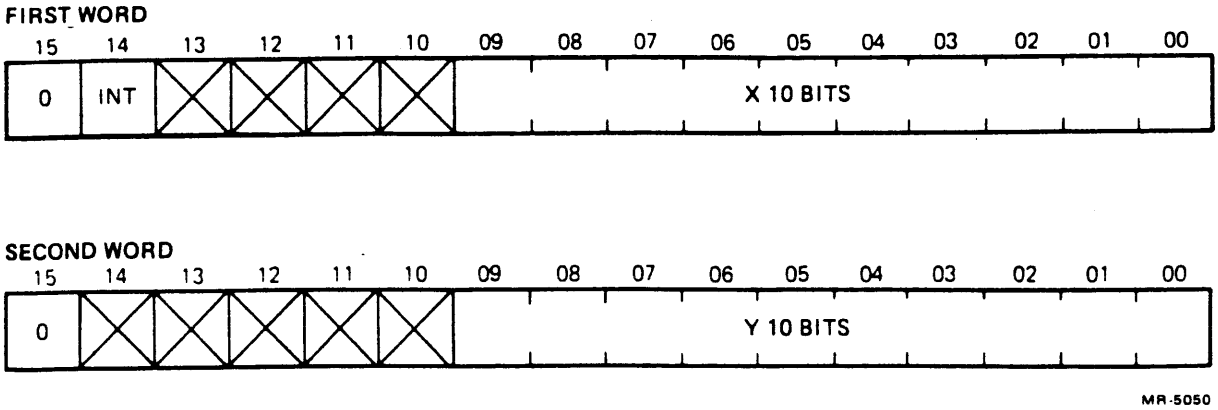


Figure 3-18
Absolute Point Data Word Format (Mode 0011)

Table 3-17
Absolute Point Data Word Definitions

	Bit	Name	Definition
1st word	15	-	0 indicates Data word
	14	INT (Intensify)	1 allows point to be written 0 causes only the Graphic Position to be updated
	13-10	Reserved	Must be written to 0
	9-0	ABSOLUTE-X Coordinate	10-bit absolute X coordinate. Bit 0 must be written to 0.
2nd word	15	-	0 indicates Data word
	14-10	Reserved	Must be written to 0
	9-0	ABSOLUTE-Y Coordinate	10-bit absolute Y coordinate. Bit 0 must be written to 0.

3.5.1.5 GRAPH/HISTOGRAM X Mode -

The Graph/Histogram X mode is used, together with Historgram Base and Graph/Histogram Increment parameters (specified by Control instructions), to draw to graph or histogram relative to the vertical axis (Y axis) on the system monitor. The associated Graphic-Data instructions, each containing an X displacement (from the Y axis) and a function code, can be used to generate the following displays, illustrated in Figure 3-19:

1. GRAPH X -- data is displayed as a series of single intensified points on the monitor.

2. CONNECTED GRAPH X -- similar to GRAPH X, but successive points are connected by a line (vector).

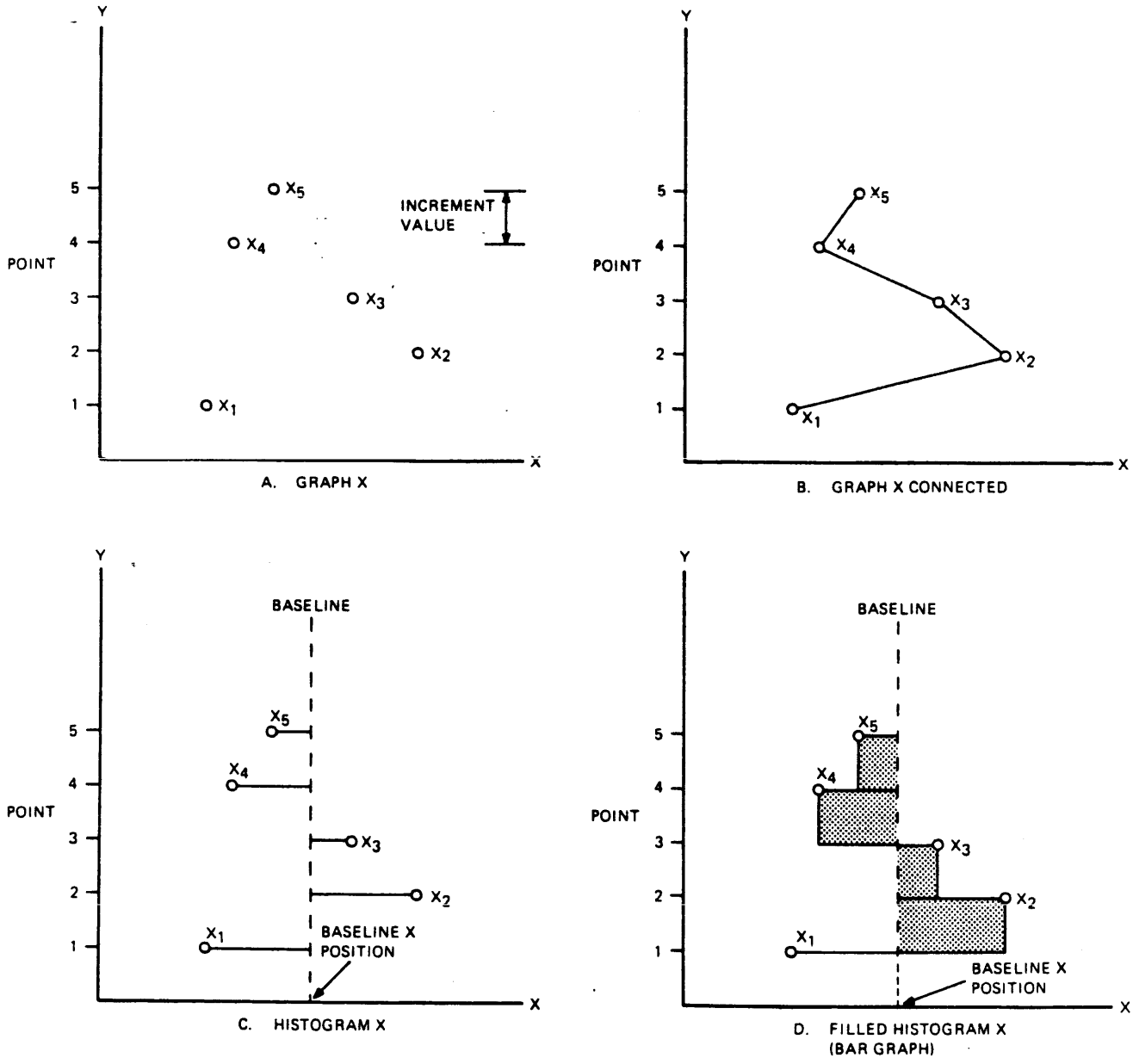
3. HISTOGRAM X -- each displayed data point is connected to the histogram baseline (a line parallel to the Y axis) by a line (vector)

4. FILLED HISTOGRAM X -- creates a bar graph by filling in the area between successive histogram lines.

The Graph/Histogram X mode is entered via a mode setting instruction with a mode code of 0100 for bits 14-11 (Figure 3-14). Pixel data for subsequent plotting is specified in bits 9-0 of the instruction (if bit 10 is 1). All plotting (points and connecting filling lines) uses the same pixel data.

The Graph/Histogram X mode instruction is followed by a number of Graph/Histogram data instructions (Figure 3-20 and Table 3-18). Bits 14 and 13 specify the plotting function to be performed. Bits 9-0 specify the plotting function to be performed. Bits 9-0 specify an absolute X coordinare. Bit 12, when set, specifies that the current Graph/Histogram Increment value is to be ignored and an increment of zero used for this point (the Y position is not stepped before plotting).

During plotting, X-coordinate positioning information is supplied explicitly from the data stream, while Y-coordinate positioning is supplied implicitly by adding the Increment parameter to the current Y position to obtain the final plot position. Note that the Increment parameter is handled as a "pre-increment" operation. This fact is most obvious in the Connected-Graph and Filled Histogram functions. In a Connected Graph, the connection line is a vector drawn from the current position to the new plot position -- the Y used for drawing the vector is the Increment value. In a Filled Histogram, the area is filled by "plotting" single-line histograms from the current Y position to (and including) the final Y position.



NOTE:
THE INITIAL Y POSITION IS EQUAL TO THE Y POSITION OF X1; THE FIRST POINT PLOTTED IN EACH GRAPH IS DISPLAYED AS DRAWN WITH THE "INCREMENT INHIBIT" BIT SET IN THE DATA WORD.

MR 5051

Figure 3-19
Graph/Histogram-X Mode Displays

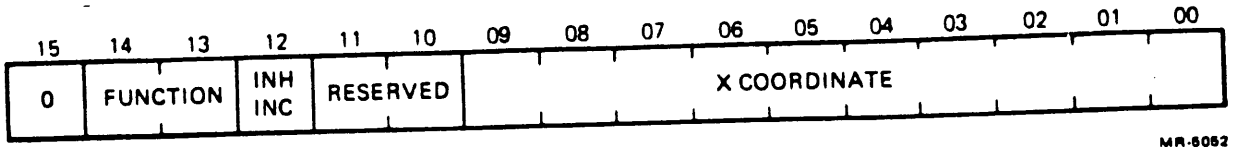


Figure 3-20
Graph/Histogram-X Data Word Format

Table 3-18
Graph/Histogram Data Word Definitions

Bit	Name	Definition
15	-	"0" specifies Graphic Data Word
14-13	FUNCTION	This field is encoded as follows: 00--GRAPH (Plot Single Point) 01--CONNECTED GRAPH (connect new point to current point) 10--HISTOGRAM (single-pixel-width line to baseline) 11--FILLED HISTOGRAM (Bargraph)
12	INH INC (Inhibit Increment)	"0" specifies that the value loaded by the LOAD GRAPH HISTOGRAM INCREMENT instruction is to be added to the current Y position before the point is plotted. "1" forces an increment value of 0 to be used (the Y position is not stepped before the new point is plotted).
11-10	Reserved	Must be written to 0.
9-0	X-COORDINATE	Absolute X-coordinate of the Graph or Histogram position to be plotted. [Note: the 10 bits of X coordinate is based on a full-screen resolution of 1024 points to allow for system expansion. In the VSV11/VS11 system of 512-point resolution, X bit 0 is reserved and should be written to 0.]

3.5.1.6 GRAPH/HISTOGRAM Y Mode -

The Graph/Histogram Y mode is used, together with the Histogram Base and Graph/Histogram Increment parameters (specified by Control instructions), to draw a graph or histogram relative to the horizontal axis (X-axis) on the system monitor. This mode is similar to the Graph/Histogram X mode, except that explicit Y data is supplied from the data instructions while the X position is stepped by the current Increment value.

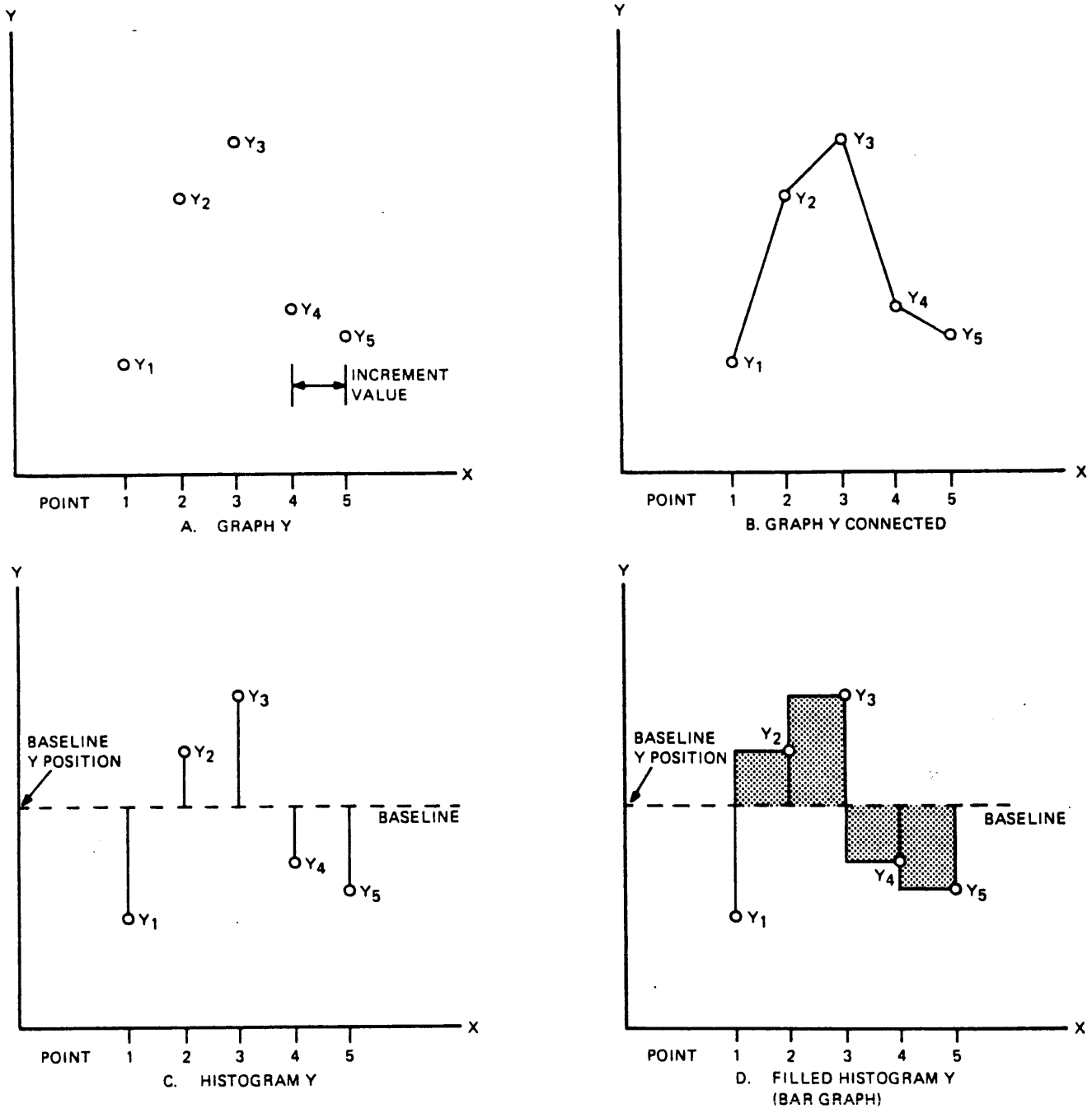
Figure 3-21 illustrates the displays generated by the Graph, Connected Graph, Histogram and Filled Histogram functions. Figure 3-22 shows the data word format for the Graph/Histogram Y mode. Table 3-19 explains the function of each bit.

3.5.1.7 RELATIVE POINT Mode -

The relative point mode is used to generate a point on the system monitor "relative" to the current graphic drawing position. The X- and/or Y-coordinates of the last display position are updated to the new display position.

A minimum of two instructions are required for the relative point mode. The first instruction sets the mode (Figure 3-14) by specifying a mode code of 0110 for bits 14-11. The intensity (for black and white systems), or color (for color systems) is specified in bits 9-0. Bit 10 must be set to a one to enable changing the current pixel data to that specified in bits 9-0.

The relative point mode instuction is followed by one or more relative point data instructions (Figure 3-23 and Table 3-20). Six bits each of the X and Y components (based on 1024-pixel screen resolution) of the new display position are specified in the data word, along with a sign bit for each component. The sign bits specify the direction of the components. Bit 14 (intensify) must be set to a one to cause Image Memory to be written (make the point visible on the system monitor or erase a previous point).



NOTE:
THE INITIAL X POSITION IS EQUAL TO THE X POSITION OF Y1; THE FIRST POINT PLOTTED IN EACH GRAPH IS DISPLAYED AS DRAWN WITH THE "INCREMENT INHIBIT" BIT SET IN THE DATA WORD.

Figure 3-21
Graph/Histogram-Y Mode Displays

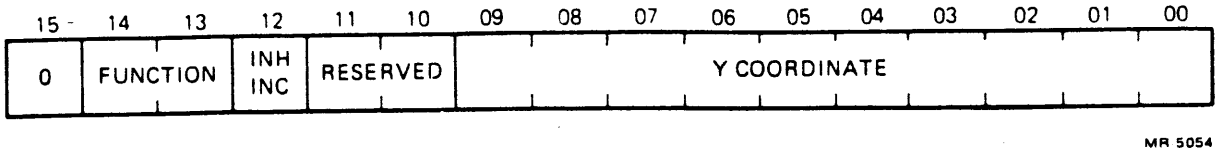


Figure 3-22
Graph/Histogram Y Data Word Format

Table 3-19
Graph/Histogram-Y Data Word Definitions

Bit	Name	Definition
15	-	"0" specifies Graphic Data Word.
14-13	FUNCTION	This field is encoded as follows: 00--GRAPH (Plot Single Point) 01--CONNECTED GRAPH (connect new point to current point) 10--HISTOGRAM (single-pixel-width line to baseline) 11--FILLED HISTOGRAM (Bargraph)
12	INH INC (Inhibit Increment)	"0" specifies that the value loaded by the LOAD GRAPH HISTOGRAM INCREMENT instruction is to be added to the current X position before the point is plotted. "1" forces an increment value of 0 to be used (the X position is not stepped before the new point is plotted).
11-10	Reserved	Must be written to 0.
9-0	Y-COORDINATE	Absolute Y-coordinate of the Graph or Histogram position to be plotted. [Note: the 10 bits of Y coordinate is based on a full-screen resolution of 1024 points to allow for system expansion. In the VSV11/VS11 system of 512-point resolution, Y bit 0 is reserved and should be written to 0.

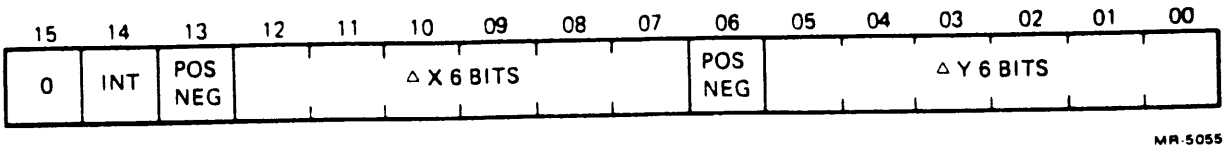


Figure 3-23
Relative-Point Data Word Format (Mode 0110)

Table 3-20
Relative-Point Data Word Field Assignments

Bit	Name	Description
15	-	0 indicates Data word.
14	INT (Intensify)	1 causes the point to be written ("intensified"); 0 causes the graphic position to be updated to the specified point, but no pixel data is written into image memory.
13	± X (Positive or Negative X)	0 specifies that the X component moves to the right (+); 1 specifies that the X component moves to the left (-).
12-7	DELTA-X	6-bit magnitude of the X (horizontal) component of the move. (Note that the LSB is reserved).
6	± Y (Positive or Negative Y)	0 specifies that the Y component moves up (+); 1 specifies that the Y component moves down (-).
5-0	DELTA-Y	6-bit magnitude of the Y (vertical) component of the move. (Note that the LSB is reserved).

3.5.1.8 RUN-LENGTH Mode -

Run-Length mode can be used to repetitively display the same pixel data (intensity) horizontally across the screen (parallel to X-axis) of the system monitor.

A minimum of two instructions are required for Run-Length mode. The first instruction sets the mode (Run-Length mode) by specifying a mode code of 1001 for bits 14-11 (refer to Figure 3-24 and Table 3-21). Bit 10 is part of the Op-code and must be a zero. Bits 8, 6 and 5 are used to control operation. Bits 9, 7 and 4-0 are unused and must be written to zeros.

One or more Run-Length Data instructions can follow the Run-Length Mode instruction. The data instruction (Figure 3-25 and Table 3-22) specifies the run length and pixel data. The 7-bit run length indicates the number of consecutive times the same pixel data will be displayed along the X-axis. The display position is automatically incremented by one along the X-axis until the count specified in the run length is reached. At the end of the run, the VSV11/VS11 requests another data word. The maximum run length that can be specified is 177 (8) [127 (10)]. A run-length field of zero is interpreted as a NEWLINE command, causing the X position to return to its original position (at the time of Run-Length mode instuction was fetched) and the Y position to be stepped up or down by one or two lines.

The pixel data bits (bits 7-0) are used to specify the intensity (for black and white systems), or color (for color systems) of the displayed pixel.

A typical display file could consist of a series of Run-Length mode data instructions, each instruction specifying a different intensity level or color for the pixel data. The pixel data can be changed with each new data word. The DSR is not updated with the new pixel data in Run-Length mode.

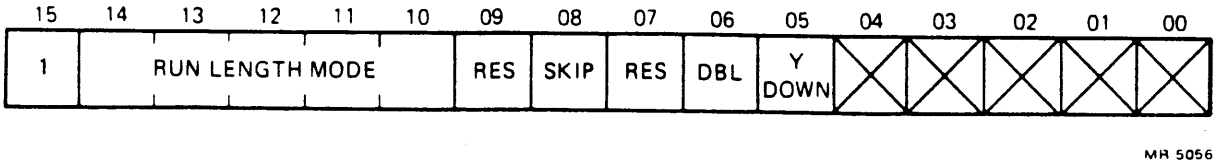


Figure 3-24
Run-Length Mode Instruction Word Format

Table 3-21
Run-Length Mode Instruction Word Definitions

Bit	Name	Description
15	-	"1" specifies Instruction word.
14-10	Run-Length Mode OpCode	"10010" specifies entry into the Run-Length Mode
9, 7, 4-0	Reserved	These bits are reserved and must be written to 0.
8	SKIP (Enable Line-Skip)	"0" specifies that the Y position is to be stepped by one pixel line on the screen when a NEWLINE data command is encountered. "1" specifies that the Y position is to be stepped by two pixel lines when a NEWLINE data command is encountered.
6	DBL (Double-Count)	"0" specifies that the Run-Length count field in the data word specifies the number of pixels to be written. "1" specifies that twice the number of pixels indicated in the Run-Length count field are to be written.
5	Y DOWN (Y Down)	"0" specifies that the Y position is stepped up (bottom to top) when a NEWLINE data command is encountered. "1" specifies that the Y position is stepped down (top to bottom) when a NEWLINE is encountered.

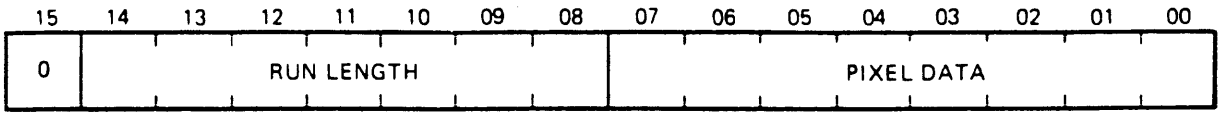


Figure 3-25
Run-Length Data Word Format

Table 3-22
Run-Length Data Word Definitions

Bit	Name	Description
15	-	"0" specifies a Graphic Data word.
14-8	RUN LENGTH	If nonzero, specifies the number of consecutive pixels to be displayed horizontally starting from the current X-Y coordinate position. (If bit 6 of the Run-Length Mode instruction was 1, twice as many pixels are written. If the Run-Length field is zero, a NEWLINE operation is performed: the X-coordinate position is restored to the value it was when the Run-Length Mode instruction was fetched, and the Y coordinate position is stepped up or down by one or two lines, as specified by bits 5 and 8 of the Mode instruction. When RUN-LENGTH=0, the Pixel Data field is ignored.
7-0	PIXEL DATA	Defines the color or intensity of the series of pixels to be written. If the RUN LENGTH field is 0, PIXEL DATA is ignored.

3.5.2 Control Instructions

The paragraphs which follow describe each of the Control instructions. These instructions provide for setup of operating parameters, display program control (No-Op, branching, stopping), and communicating with control and status registers on the Image Memory and Sync (Joystick) channels.

The Control instructions do not change the Graphic mode of the VSV11/VS11 and may be embedded within the graphic data stream of the display file. They may not, however, be inserted between the two word of a long-format graphic data packet (absolute point or long vector).

3.5.2.1 JOYSTICK STATUS -

The JOYSTICK STATUS instruction is shown in Figure 3-26 and described in Table 3-23. This instruction is used to select one out of a possible four Sync/Joystick channels which a VSV11/VS11 system may have, to control cursor crosshair intensity (on or off), retrieve cursor X-Y coordinates and status, and enable Cursor Match and Joystick Switch interrupts.

Bits 14-10 contain the op-code (10011) for the JOYSTICK STATUS instruction. The Joystick Select bits (bits 8 and 9) are used to select one out of four possible channels. In a multi-joystick system, the joysticks are addressed 0, 1, 2, 3. If the Channel Protect bit in the CSR register is set, the Joystick Select bits are ignored and the joystick channel number is supplied from CSR bits 8 and 9.

Joystick 0 is selected by writing zeros to bits 8 and 9. Joystick 1 is selected by writing bit 8 to a one and bit 9 to a zero. The remaining two joysticks (2 and 3) are selected by writing bits 8 and 9 to 10 and 11 respectively. It should be noted that only one joystick can be selected at one time. The selected joystick overrides the non-selected joysticks. In a single joystick system, the joystick is addressed as 0.

Bit 7 is an unused bit and must be written to zero.

Bits 5 and 4 control the cursor crosshair intensity. Both of these bits must be written to a one to intensify (make visible) the cursor crosshairs. In order to turn off the cursor intensity, bit 5 must be set to 1 while bit 4 is set to 0.

The Match Interrupt Enable (bit 3) and the Match Interrupt (bit 2) control the Cursor Match interrupt. This interrupt to the Display Processor is produced when the cursor X-Y coordinates are the same (match) as an Image Memory pixel position (X-Y coordinates) being written when the joystick interrupt switch is pressed (or when the "simulated joystick switch" is active, see Paragraph 3.5.2.2). The Display Processor must be writing to the

Image Memory pixel location which matches the X-Y cursor coordinates. At the time the match interrupt to the host occurs, the X-Y coordinates of the cursor position are in the Display Processor's DXR and DYR status registers.

Bits 1 and 0 control the switch interrupt. This interrupt is produced whenever the joystick interrupt switch is pressed (or the "simulated switch" is active) and the VSV11/VS11 has finished processing an instruction. Both bits (bits 1 and 0) must be written to a one to enable the interrupt. When the interrupt is produced, if the DPU was running, the X-Y coordinates of the cursor, plus various status bits, are in the Display Processor DXR and DYR status registers (Paragraphs 3.3.3 and 3.3.4). If the DPU was idle, the program must request that the cursor position and status be retrieved.

When bit 6 is coded to 1, the cursor X-Y coordinates and various status bits (Crosshair Intensity Enable, Match and Switch Interrupt Enables, and Interlace/Noninterlace Status) are retrieved from the selected channel and placed in the DXR and DYR registers (Paragraphs 3.3.3 and 3.3.4.)

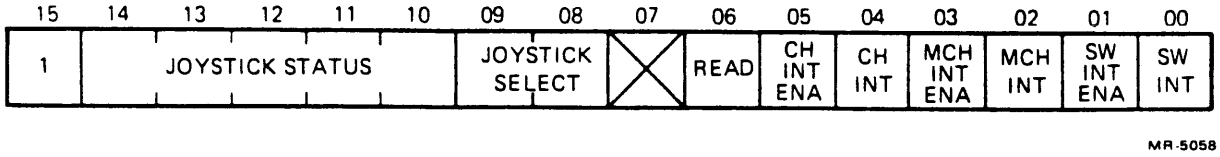


Figure 3-26
JOYSTICK STATUS Instruction Format

Table 3-23
JOYSTICK STATUS Instruction Bit Definitions

Bit	Name	Description
15	-	"1" indicates Control word.
14-10	Op-Code	"10011" specifies the JOYSTICK STATUS Control instruction.
9-8	JOYSTICK SELECT	Addresses one of four possible joystick channels to receive the data specified in bits 6-0.
7	Reserved	Must be written with 0.
6	READ (Read Cursor)	When set (1), this bit causes the current X-Y cursor coordinates, along with various status bits, to be retrieved from the selected channel and displayed in the DXR and DYR registers. The information in DXR and DYR is lost on succeeding graphic drawing operations. When this bit is clear (0), no read operation occurs.
5	CH INT EN (Crosshair Intensity Enable)	When set (1), enables CROSSHAIR INTENSITY (bit 4) to be loaded into the intensity register.
4	CH INT (Crosshair Intensity)	1 = Crosshair Intensity On 0 = Crosshair Intensity Off [This bit has meaning only if bit 5, CH INT EN, is set (1).] The CH INT status can be read in bit 12 of the DYR register following retrieval of cursor coordinates.
3	MCH INT ENA (Match Interrupt Enable)	When set (1), enables MATCH INTERRUPT (bit 2) to be loaded into the Match Interrupt register to enable or disable the Match Interrupt.
2	MCH INT (Match Interrupt)	1 = enable Cursor Match Interrupt 0 = disableCursor Match Interrupt [This bit has meaning only when bit 3, MAT INT EN, is set (1).]

Table 3-23 (con't)
JOYSTICK STATUS Instruction Bit Definitions

Bit	Name	Description
2	MCH INT (con't)	When the Match Interrupt is enabled, the Display Processor is interrupted out of a graphic drawing operation when the current pixel writing position matches the cursor position. This "matching" position is displayed in the DXR and DYR registers, but the actual graphic position, stored internally, is updated to the logical endpoint of the graphic operation. The state of MAT INT can be read as bit 12 of the DXR register following retrieval of cursor coordinates.
1	SW INT ENA (Switch Interrupt Enable)	When set (1), this bit enables the SWITCH INTERRUPT bit, bit 0, to be loaded into the joystick channel to enable or disable the Switch Interrupt.
0	SW INT (Switch Interrupt)	1 = enable Switch Interrupt 0 = disable Switch Interrupt [This bit has meaning only if bit 1, SW INT EN, is set (1).] When the Switch Interrupt is enabled, the Joystick Switch Interrupt request is posted to the host computer when the joystick switch is pressed. If the DPU is running when the switch is pressed, display file processing stops at the end of the current instruction and the cursor X-Y coordinates are loaded into the DXR and DYR registers. If the DPU is idle when the switch is pressed, only the interrupt occurs; the program must request the coordinates to be retrieved (Paragraph 3.3.3). The state of SW INT can be read as bit 11 of the DXR register following retrieval of cursor coordinates.

3.5.2.2 LOAD EXTENDED JOYSTICK CONTROL -

The LOAD EXTENDED JOYSTICK CONTROL instruction, shown in Figure 3-27 and described in Table 3-24, controls the hardware blink feature and allows the display program to simulate the closing of the manual Joystick Interrupt Switch.

Bits 14-8 of the instruction word define the Op-code of the instruction and must be coded to 1111011. The basic instruction word is therefore 175400 (octal).

Bits 7-6 specify the joystick channel to be loaded (if the Channel Protect bit in the CSR is zero). If the Channel Protect bit in the CSR is one, instruction bits 7-6 are ignored and the channel number is supplied from CSR bits 9-8.

Bits 5-2 are reserved. They are transmitted to the selected joystick channel but have no effect.

Writing a 1 into bit 1 simulates closure of the manual joystick switch; writing a 0 releases the simulated switch. The simulated switch can be used with the interrupt enable bits in the Joystick Status instruction to cause Switch and Match interrupts.

Bit 0 controls the pixel Blink Enable in the joystick channel. Writing a 0 into this bit enables the blink feature. When blinking is enabled, any pixel displayed from the selected channel will blink (flash off and on) if it contains a 1 in Video-Bus Data bit 6 (least- significant bit of GREEN in color systems). This bit corresponds to bit 8 of the pixel data supplied in the Graphic-Mode instruction words. Writing a 0 into bit 0 disables the blink feature.

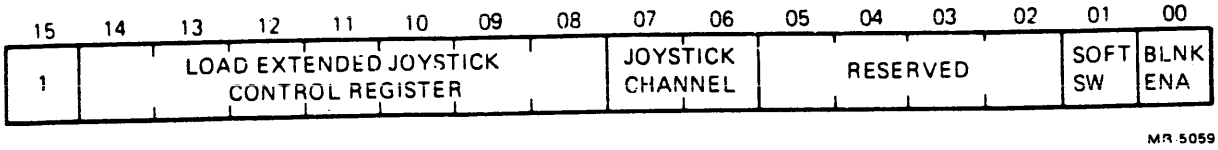


Figure 3-27
LOAD EXTENDED JOYSTICK CONTROL Instruction Format

Table 3-24
LOAD EXTENDED JOYSTICK CONTROL Instruction Bit Definitions

Bit	Name	Description
15	-	1 indicates Control word.
14-8	Op-Code	"1111011" specifies the LOAD EXTENDED JOYSTICK CONTROL REGISTER instruction.
7-6	JOYSTICK CHANNEL	Addresses one of four joystick channels to receive the data in bits 5-0.
5-2	Reserved	Should be written to 0.
1	SOFT SW (Simulate Switch)	When set (1), causes simulated closure of the manual joystick switch. When clear (0), the simulated switch is released. (The simulated switch is inclusively-ORed with the manual switch input.
0	BLNK ENA (Blink Enable)	When set (1), enables the blink feature (pixels with bit 8 set blink on and off). When clear (0), disables the blink feature.

3.5.2.3 WRITE CURSOR COORDINATES -

The WRITE CURSOR COORDINATES control instruction, shown in Figure 3-28 and described in Table 3-25, loads the X and Y cursor coordinate registers in the selected joystick channel with the data from the following two words of the display file. Ten significant bits of each coordinate are sent to the channel, allowing the program to place the cursor outside of the visible screen area if the most-significant bit (bit 10) of either coordinate is one.

This instruction allows the program to set up initial cursor coordinates or simulate the action of the manual joystick.

Bits 7 & 6 of the instruction word select the joystick channel (if the Channel Protect bit in the CSR is zero).

Bits 5-0 of the instruction word are ignored but are reserved for future expansion.

The coordinate data in the second and third instruction words is placed in the same format as that used by the Graphic Mode instructions (based on a full-screen resolution of 1024 points).

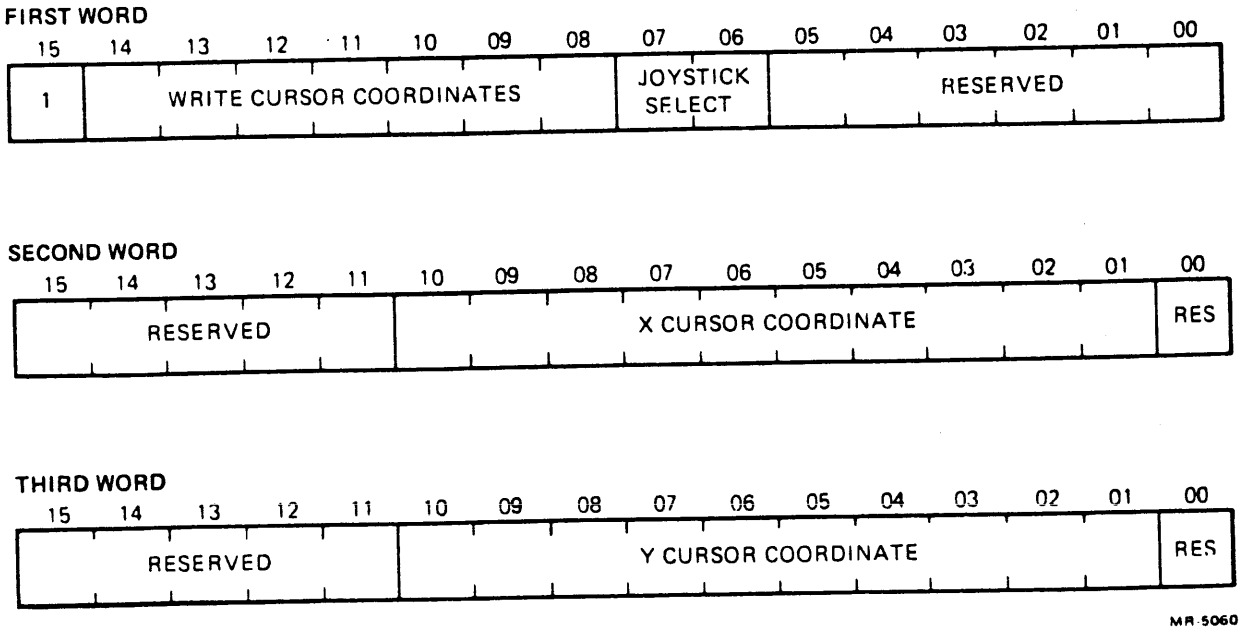


Figure 3-28
WRITE CURSOR COORDINATES Instruction Format

Table 3-25
WRITE CURSOR COORDINATES Instruction Bit Definitions

	Bit	Name	Description
1st Word	1	-	1 indicates Control word.
	14-8	Op-Code	"1111010" specifies the WRITE CURSOR COORDINATES instruction.
	7-6	JOYSTICK SELECT	Addresses one of four joystick channels to receive the cursor coordinate data in the following two words.
	5-0	Reserved	Must be written to 0.
2nd & 3rd Words	15-11	Reserved	Must be written to 0.
	10-0	X/Y CURSOR COORDINATES	Words 2 and 3 specify the X and Y cursor coordinate data, respectively. The data is in the standard format for the 1024-point resolution. In the VSV11/VS11 system of 512-point resolution, bit 0 of each coordinate is unused and should be written with 0. If bit 10 of either coordinate is set (1), the cursor is placed outside of the visible screen area.

3.5.2.4 SET HISTOGRAM BASE -

The SET HISTOGRAM BASE control instruction is used to establish a baseline position for a histogram or filled-histogram (bargraph). This instruction is usually issued before the Graph/Histogram X or Graph/Histogram Y graphic mode instructions.

As shown in Figure 3-29 and Table 3-26, the SET HISTOGRAM BASE instruction is a two-word instruction. The first word specifies the Op-code in bits 14-10; bits 9-0 are reserved and should be set to 0.

The second word of the instruction specifies the coordinate location of the histogram baseline. The baseline position is interpreted within the context of the GRAPH/HISTOGRAM instruction subsequently executed: for GRAPH/HISTOGRAM-X mode, the baseline is parallel to the Y axis; for GRAPH/HISTOGRAM-Y mode, the baseline is parallel to the X axis. [There is only one Histogram Base register.] The position information is in the standard format for graphic coordinate data (based on a full-screen resolution of 1024 points).

After the histogram baseline coordinate is fetched, it is shifted one place to the right and stored in bits 11-0 of the internal HBASE register, which can be read via the DSR (Paragraph 3.3.2).

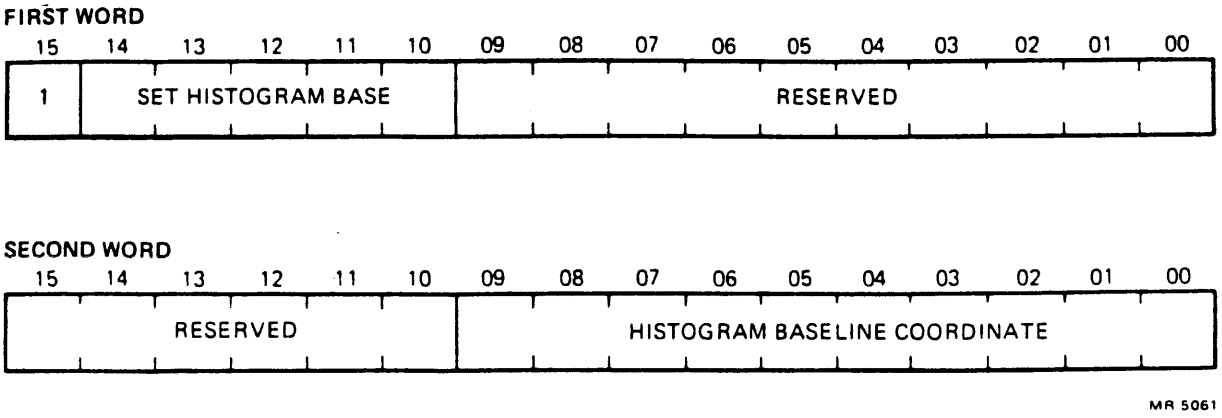


Figure 3-29
SET HISTOGRAM BASE Instruction Format

Table 3-26
SET HISTOGRAM BASE Instruction Bit Definitions

	Bit	Name	Description
1st Word	15	-	1 indicates Control word
	14-10	Op-Code	"10100" specifies the SET HISTOGRAM BASE instruction Op-Code.
	9-0	Reserved	Must to be written to 0.
2nd Word	15-10	Reserved	Must be written to 0.
	9-0	HISTOGRAM BASELINE COORDINATE (Position)	Location of the histogram baseline. This coordinate is based upon a full-screen resolution of 1024 points; in the VSV11/VS11 system of 512 points, bit 0 is not used and should be set to 0.

3.5.2.5 SET CHARACTER BASE -

The SET CHARACTER BASE control instruction is used to establish the base address of the table of dispatch addresses used in character mode. This instruction must be issued before using the Character Mode instruction. Once set, the character base address remains unchanged until the VSV11/VS11 is initialized or until another Set Character Base instruction is issued.

As shown in Figure 3-30 and Table 3-27, the SET CHARACTER BASE instruction is a two-word instruction. The first word specifies the Op-code. Bits 15-1 of the second word specify the virtual display file address of the character dispatch table; bit 0 of this word selects the display file segment (0 indicates that the table is in the Main file segment, while 1 indicates that it is in the Auxiliary segment). The dispatch table and associated character drawing routines must reside in the same segment. The base address is added to the character code in a Character Mode data word (Paragraph 3.5.1.1). The resultant (virtual) address is a pointer (indirect address) to the starting location of a character dispatch routine. For example, assume a character base of 2000 (8) and the character E is to be drawn. The following occurs:

1. Character base = 2000 (8)

2. Character E = 105 (8) ASCII = 001 000 101

3. VSV11/VS11 microcode shifts character code one place the left - 010 001 010 = 212 (8). (The one place shift is done because the VSV11/VS11 can only address even locations).

4. Add character base and shifted character code -

   ```
   2000 (8)
   +212 (8)
   ----
   2212 (8) = 010 010 001 010
   ```

5. 2212 (8) is the memory location the VSV11/VS11 Display Processor will go to. The contents of 2212 (8) will contain a number that is the address of the character drawing routine. The first word of the routine must be either a Graphic Mode instruction or Control instruction, but not data. The character mode instruction will therefore enter a display file that is used to describe a "picture". The POP instruction (Paragraph 3.5.2.8) must be used at the end of the display file to return the Display Processor to the main routine. It is illegal to enter the character mode while the VSV11/VS11 is performing a character draw routine.

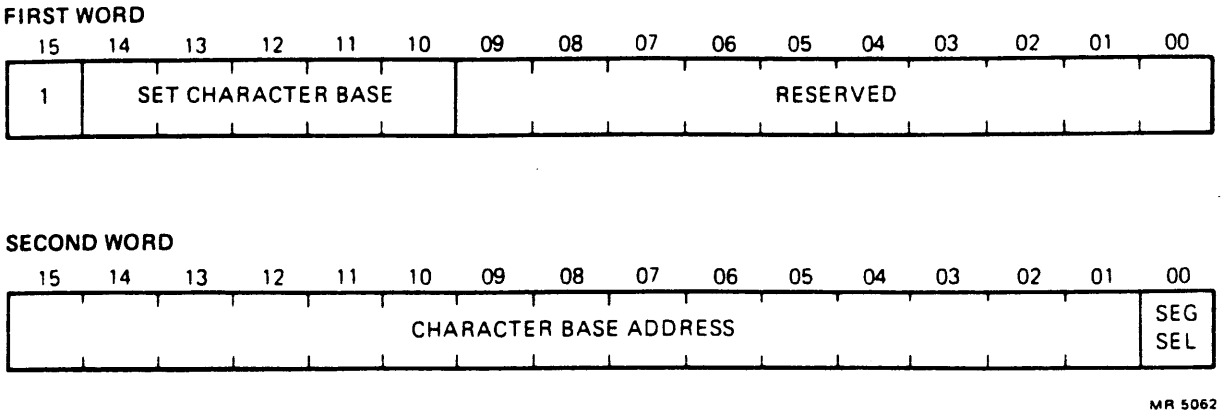


Figure 3-30
SET CHARACTER BASE Instruction Format

Table 3-27
SET CHARACTER BASE Instruction Bit Definitions

	Bit	Name	Description
1st Word	15	-	1 indicates Control word
	14-10	Op-Code	"10101" specifies the SET CHARACTER BASE instruction
	9-0	Reserved	Must to be written to 0.
2nd Word	15-1	CHARACTER BASE ADDRESS	Virtual address of the first location in a block of words containing the addresses of character drawing subroutines. These addresses refer to locations within the segment specified in bit 0 (SEG) of the instruction word.
	0	SEG SEL (Segment-Select)	"0" specifies that the dispatch table and associated character- drawing routines reside in the Main display file segment. "1" specifies that the table and routines reside in the Auxiliary segment.

3.5.2.6 DISPLAY JUMP -

The DISPLAY JUMP (DJUMP) control instruction is used to perform a "jump" to a virtual address within the current display file segment. This instruction is a two-word instruction, as shown in Figure 3-31 and Table 3-28. The Op-code (160000 (8)) is specified in the first word. The virtual destination address of the jump is specified in the second word. Because the VSV11/VS11 is a word-oriented machine and because jumping is allowed only within the current display-file segment, bit 0 of the second word must be 0.

Because jumping is allowed only within the current segment, display subroutines (such as for drawing characters) that are assembled to run in one segment and include jumps can be run in the other display-file segment without reassembly.

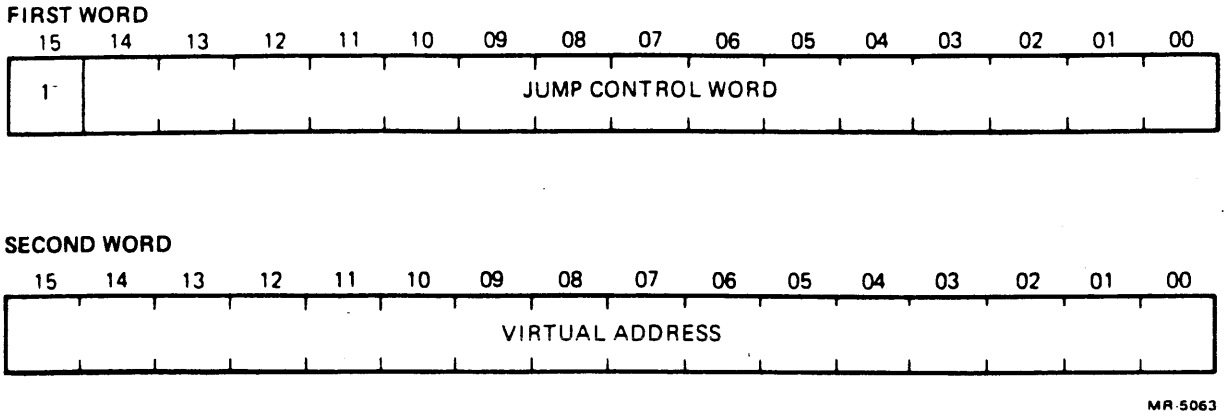


Figure 3-31
DISPLAY JUMP Instruction Format

Table 3-28
DISPLAY JUMP (DJUMP) Instruction Bit Definitions

	Bit	Name	Description
1st Word	15	-	1 indicates Control word
	14-0	Op-Code	160000 (8) specifies the DISPLAY JUMP instruction Op-Code.
2nd Word	15-1	VIRTUAL JUMP ADDRESS	Specifies the destination address of the jump instruction.
	0	-	The address is a word address in host memory within the current display file segment; this bit must therefore be 0.

3.5.2.7 DISPLAY JUMP-TO-SUBROUTINE -

The DISPLAY JUMP-TO-SUBROUTINE (DJMS) control instruction is used to call a display subprogram. It functions a similarly to the Character Mode subroutine call but provides for a "direct" call to the subroutine. The subroutine can reside in either the Main or Auxiliary display-file segment and must be terminated with a DPOP instruction to return the display program to the Main segment at the location following the DJMS instruction. Only one level of subroutining is allowed.

As shown in Figure 3-32 and Table 3-29, DJMS is a two-word instruction. The first word specifies the Op-code (160001 octal). Bits 15-1 of the second word specify the virtual display file address of the subroutine being called. Bit 0 of the second word specifies the segment for the address (0 specifies Main segment, 1 specifies Auxiliary segment).

Only one level of subroutining is allowed, which implies:

1. The DJMS cannot be executed from a subroutine (either one called via the Character mode or by another DJMS).

2. DJMS cannot be executed from the Auxiliary segment (since a subroutine call is required in order to begin execution in the Auxiliary segment.

3. The Bit-Map and DMA Pixel Readback instructions cannot be executed within a display subroutine (since these instructions use the address-save register in the VSV11/VS11.

If an attempt is made to violate any of the above restrictions, display processing stops with a Sequence Error.

If processing is stopped within a display subroutine, the internal PCSAVE register (accessed via DSR) contains the virtual address of the instruction following the DJMS.

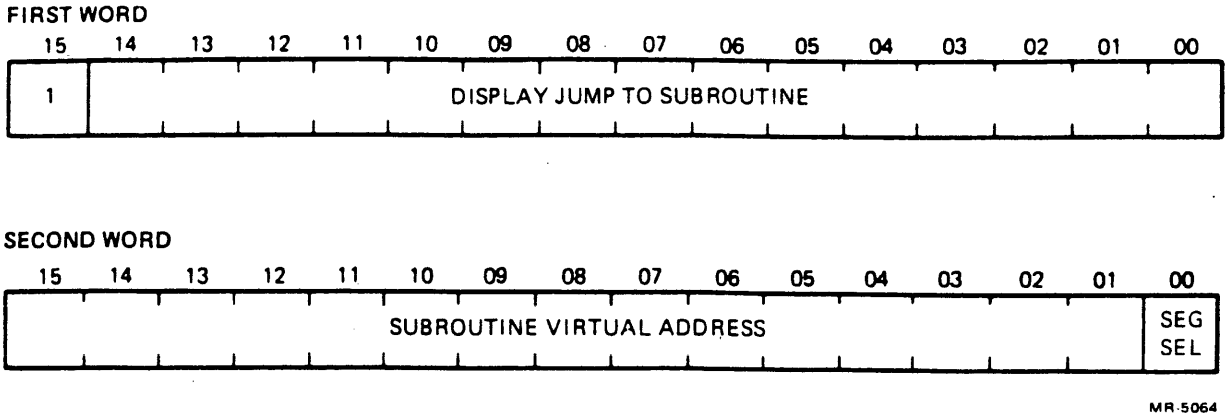


Figure 3-32
DISPLAY JUMP-TO-SUBROUTINE Instruction Format

Table 3-29
DISPLAY JUMP-TO-SUBROUTINE (DJMS) Instruction Bit Definitions

	Bit	Name	Description
1st Word	15	-	1 indicates Control word
	14-0	Op-Code	160001 (8) specifies the DISPLAY JUMP-TO-SUBROUTINE Op-Code.
2nd Word	15-1	SUBROUTINE VIRTUAL ADDRESS	Specifies the destination address of the DJMS instruction.
	0	SEG SEL (Segment Select)	Specifies the display file segment of the subroutine: "0" = Main Segment "1" = Auxiliary Segment

3.5.2.8 DISPLAY POP -

The DISPLAY POP (DPOP) control instruction is used to return from a display subroutine (one called either by DJMS or via the Character mode).

DPOP is a single-word instruction, shown in Figure 3-33 and Table 3-30. It is coded as 165000 (octal).

When DPOP is executed, the Display Program Counter (DPC) is loaded with the contents of the PCSAVE register (containing the return address) and the Main segment memory management parameters are restored, thereby returning the display program to the location following the original subroutine call (either a DJMS or a Character mode data word). Bit 0 of PCSAVE (accessible via the DSR) is then set to 1 to indicate that it is "empty" and can be used for another subroutine call.

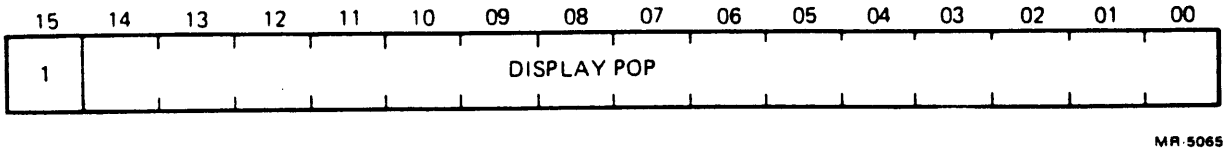


Figure 3-33
DISPLAY POP Instruction Format

Table 3-30
DISPLAY POP (DPOP) Instruction Bit Definitions

Bit	Name	Description
15	-	"1" indicates Control word
14-0	Op-Code	Octal 165000 for the word specifies the DISPLAY POP instruction.

3.5.2.9 DNOP -

The DISPLAY NOP (DNOP) instruction is used to place the Display Processor into a stall.

As shown in Figure 3-34 and Table 3-31, the DNOP control instruction is a single word instruction. The DNOP op-code (110100) is specified in bits 14-9. A vertical down count is specified in bits 8-0. The VSV11/VS11 will do NOPs for the number of vertical syncs specified in ther vertical down count. If the vertical down count equals zero, a NOP will occur for one DPU instruction cycle. After the NOP, the Display Processor will continue to the next instruction.

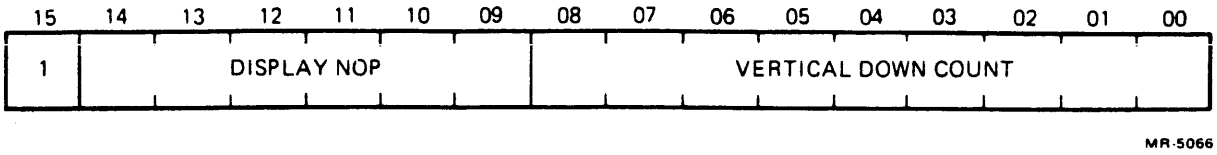


Figure 3-34
DNOP Instruction Word Format

Table 3-31
DNOP Instruction Bit Definitions

Bit	Name	Description
15	-	"1" indicates Control word
14-9	Op-Code	"110100" specifies the DNOP instruction. The DPU will "stall" for the number of vertical sync's specified by the Vertical Down Count bits (bits 8-0). If the count is 0, no stall occurs; the DPU proceeds on to the next instruction.
8-0	VERTICAL DOWN COUNT	Specifies the number of CRT fields (vertical blank pulses) to be counted before the DPU continues to the next display instruction. Vertical sync pulses occur at 16.7 mS (60 Hz) or 20 mS (50 Hz) intervals.

3.5.2.10 LOAD STATUS REGISTER A -

The LOAD STATUS A control instruction performs several functions:

- Stopping the DPU,
- Enabling or disabling the STOP interrupt,
- Switching the Image Memory Read/Write mode, and
- Clearing or setting enabled image memories.

As shown in Figure 3-35 and Table 3-32, the LOAD STATUS A instruction is a single-word instruction. The op-code for the instruction is specified in bits 14-11. Bits 10, 9 and 8 set up the DPU stop function. If bit 10 is set, and bits 8 and 9 are zeros, the DPU will stop and no stop interrupt will be produced. The DPU will stop and a stop interrupt will be generated if bits 10, 9 and 8 are all set to ones. Bits 9 and 8 enable or disable the stop interrupt. The actual interrupt enable is stored internally and could be in the set state ("1" state) from a previous LOAD STATUS A instruction. With bits 10, 9 and 8 controlling the stop function, it is possible to:

1. Stop the DPU and not generate an interrupt,
2. Set the internal Stop Interrupt Enable and not perform a stop, and
3. Do a stop and generate a STOP interrupt to the CPU.

Bit 7 is the Image Memory "Switch" bit. For each memory channel to be switched, this function must be enabled with the Read/Write Switch Enable bit (bit 3) of the LOAD STATUS C control instruction (Paragraph 3.5.2.11). Since the Image Memory is a single port memory, the port is multiplexed for read and write operations. If the Image Memory has been selected for Read-Only (Paragraph 3.5.2.11, bits 4 and 5), and new pixel data is now going to be written to the memory, setting bit 7 to a one will cause bits 4 and 5 of the data loaded by the LOAD STATUS C instruction to be swapped. This places the Image Memory in the Write-Only mode. Before the Image Memory can be read for display, another switch must occur after the memory write. In a multi-image memory system, the Switch bit can control the switching between two memories. Thus, one memory can be read while the other is being written. This provides for smooth dynamic graphics on the system monitor.

Bits 5 and 6 are used to set or clear all write-enabled image memory planes. The memory planes are write-enabled with the LOAD STATUS C instruction. If the memory planes are write enabled, setting bits 5 and 6 to ones cause all locations of the write enabled memory planes to be cleared. Setting bit 6 to a one and

bit 5 to a zero causes all write enabled memory planes to be written with the contents of the image memory Data Latch. The Data Latch may contain pixel data from a previous instruction.

Bits 4-0 are not used by the Display Processor, but are available to the programmer. These bits can be used to identify various stops in the display file for programmer applications.

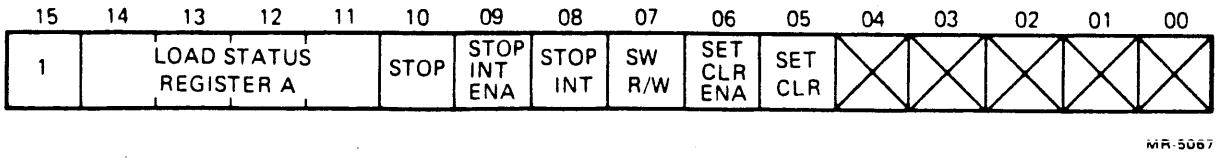


Figure 3-35
LOAD STATUS A Instruction Format

Table 3-32
LOAD STATUS A Instruction Bit Definitions

Bit	Name	Description
15	-	"1" indicates Control word.
14-11	Op-Code	"1110" specifies the LOAD STATUS A instruction.
10	STOP	When set (1), halts display file execution. After the stop, DPC is pointing to the instruction following the LOAD STATUS A.
9	STOP INT ENA (Stop Interrupt Enable)	When set, enables bit 8, STOP INTERRUPT, into the Stop Interrupt Enable register, to enable or disable the Stop interrupt.

(cont'd on next page)

Table 3-32 (con't)
LOAD STATUS A Instruction Bit Definitions

Bit	Name	Description
8	STOP INT (Stop Interrupt)	When bit 9 is 1, this bit operates as follows: "1" causes an interrupt to host CPU when display processing stops; "0" specifies that no interrupt is to occur when display processing stops. [Note: The FSI bit in CSR can force a Stop interrupt irrespective of the states of bits 9 & 8.]
7	SW R/W (Switch Read/Write Modes)	When set, causes the Read Mode and Write Mode bits in all memory channels enabled for a switch (by the LOAD STATUS C instruction) to be swapped. An enabled Read-Only memory will switch to Write-Only mode, and vice-versa. Memories in Protect mode or in Read/Write mode, or not enabled for a switch, will not be affected.
6	SET/CLR ENA	When set causes all image memories in Write-Only or Read/Write mode to be cleared or set, as specified by bit 5.
5	SET/CLR	When bit 6, SET/CLR ENA, is set, this bit controls memory action as follows: "1" causes all pixels in write-enabled memories to be cleared to zero. "0" causes all pixels in write-enabled memories to be set to the data currently in the memory Data Latch (as loaded via a Graphic-Mode or Bit-Map instruction).
4-0	Not Used	These bits are not used by the VSV11/VS11 system. They need not be written to 0 and are available for user applications.

3.5.2.11 LOAD STATUS C -

Image memory Channel Select, memory Read/Write Select, memory Switch Enable, and Pixel Mode select are the functions set-up by the LOAD STATUS C control instruction.

The LOAD STATUS C instruction is a single-word instruction, as shown in Figure 3-36 and Table 3-33. Bits 14-10 are the Op-Code bits (11111). Channel Select bits 9 and 8 are used to select a particular Image Memory channel to receive the data in bits 5-0. A typical VSV11/VS11 system can have from one to four memory channels. The channels are addressed as 0, 1, 2, and 3. A single channel system has a channel address of 0. Channel 0 is selected by writing bits 9 and 8 to zeros. Writing bits 9 and 8 to zero and one, respectively, selects channel one. The remaining two Image Memory channels are selected by setting bit 9 to a one and bit 8 to a zero (channel 2), or both bits 9 and 8 to ones (channel 3). (The Channel Select bits can be overridden by the Channel Protect bit in CSR).

Bits 7 and 6 are unused and must be written to zeros.

The memory Read/Write mode bits (5 and 4) control the read/write accessibility of the selected Image Memory. These two bits establish Read/Write modes as follows:

1. 00 = read and write both inhibited (Protect mode),
2. 01 = write enabled and read inhibited (Write-Only mode),
3. 10 = read enabled and write inhibited (Read-Only mode),
4. 11 = both read and write enabled (Read/Write mode).

Read/Write Switch Enable (bit 3) is used in conjunction with bit 7 (SW R/W) of the LOAD STATUS A instruction. When bit 3 (Read/Write Switch Enable) is set ("1" state), bits 5 and 4 of the data sent by the LOAD STATUS C instruction will switch, to change between Read and Write modes for the Image Memory.

Bits 2 and 1 control the pixel writing mode. Changing of the pixel mode is enabled when bit 2 is set ("1" state). Bit 1 controls the pixel mode. When bit 1 = 0, new data written to an Image Memory pixel location replaces existing data in that location. When bit 1 = 1, new data written to an Image Memory location is logically ORed with existing data in that location. (This function also works when setting or clearing image memories, allowing only bits selected by 1's in the Data Latch to be affected).

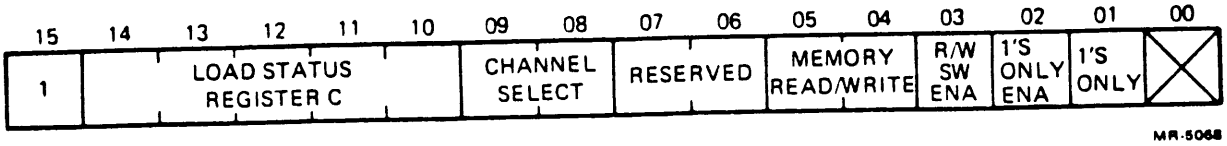


Figure 3-36
LOAD STATUS C Instruction Format

Table 3-33
LOAD STATUS C Instruction Bit Definitions

Bit	Name	Description
15	-	"1" indicates Control word.
14-10	Op-Code	"11111" specifies the LOAD STATUS C instruction.
9-8	CHANNEL SELECT	Addresses one of four Image Memory channels to receive th data in bits 5-0 of the instruction.
7-6	Reserved	Must be written to 0.
5	RD EN (Read Enable)	When set, enables the selected memory channel to be read out to the associated monitor. When clear, disables the memory from sending data to the monitor.
4	WRT EN (Write Enable)	When set, enables the selected memory channel to be written with pixel data from the DPU. When clear, disables the memory from being written. Bits 5 & 4 considered together place the memory in the following modes: 00 = PROTECT mode 01 = WRITE-ONLY mode 10 = READ-ONLY mode 11 = READ/WRITE mode Any memory in Write-only or Read/Write mode will send data to the DPU during Pixel Readback operations.

(cont'd on next page)

Table 3-33 (con't)
LOAD STATUS C Instruction Bit Definitions

Bit	Name	Description
3	R/W SW EN (Read-Write Switch Enable)	When set, enables bit 7 of the LOAD STATUS A instruction to cause the READ and WRITE mode bits in the memory channel to be swapped (READ is loaded into the WRITE bit, and vice versa).
2	1's ONLY ENA (Write 1's Only Enable)	When set, enables bit 1, 1's ONLY, to be loaded into the selected memory channel.
1	1's ONLY (Write 1's Only)	This bit, when loaded into the memory channel when bit 2 is set, controls the writing of pixel data as follows: "0" = new pixel data written to a pixel location will replace existing data in that location. "1" = new pixel data written to a pixel location will be logically ORed with the existing data (e.g., only 1's are written).
0	Reserved	Must be written to 0.

3.5.2.12 LOAD GRAPHPLOT INCREMENT -

The LOAD GRAPHPLOT INCREMENT control instruction sets up the increment (spacing) between data points plotted by the Graph/Histogram graphic mode instructions.

As shown in Figure 3-37 and Table 3-34, LOAD GRAPHPLOT INCREMENT is a single-word instruction. The instruction op-code (111100001) is specified in bits 14-6 and the increment is specified in bits 5-0.

The increment value is specified in the 1024-point resolution format (bit 0 is not used). Therefore, increments of 0 through 31 (decimal) pixels may be specified.

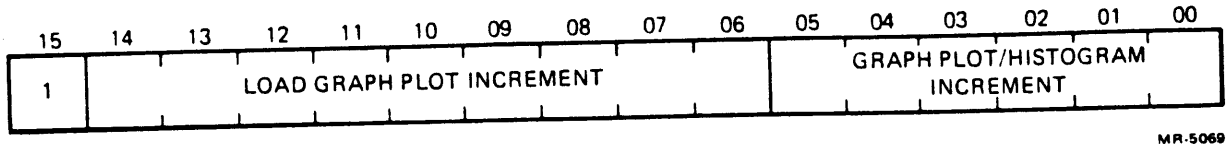


Figure 3-37
LOAD GRAPHPLOT INCREMENT Instruction Format

Table 3-34
LOAD GRAPHPLOT INCREMENT Instruction Bit Definitions

Bit	Name	Description
15	-	"1" indicates Control word.
14-6	Op-Code	"111100001" specifies the LOAD GRAPHPLOT INCREMENT instruction.
5-0	GRAPH/ HISTOGRAM INCREMENT	Sets the distance between data points executed in the Graph/Histogram-X and -Y graphic modes. The increment is specified in the 1024-point resolution format, so bit 0 is reserved and should be set to 0.

3.5.2.13 LOAD PIXEL-DATA INHIBIT -

The LOAD PIXEL-DATA INHIBIT control instruction is used to override the effect the Pixel-Data-Enable bit (bit 10) of the Graphic Mode instructions.

As shown in Figure 3-38 and Table 3-35, LOAD PIXEL-DATA-INHIBIT is a single-word instruction. Bits 14-8 along with bit 6 specify the Op-Code. Bit 7 specifies the state of the inhibit (0 to clear it, 1 to set it). Bits 5-0 of the instruction are reserved and should be set to 0.

When the inhibit (an internal flag bit within the Display Processor) is set, new pixel data is not loaded into the DSR and memory data latch by a Graphic Mode instruction, even if bit 10 of that instruction is set (1). When the inhibit is clear, the Graphic Mode instructions cause new pixel data to be loaded from bits 9-2 if bit 10 is set.

Therefore, the clear and set instructions are (in octal):

174000	clears the Pixel Data Inhibit
174200	sets the Pixel Data Inhibit

The Pixel Data Inhibit is automatically cleared on a display START but left intact on a RESUME.

The Pixel Data Inhibit feature is useful for selectively "erasing" complex pictures drawn by display files containing several changes of pixel data. Rather than having the software scan the display file and change each occurrence of pixel data specification (to black or a background color), the background pixel color/intensity needed for erasing can be set once (as, with an Absolute Point mode instruction), the Pixel-Data-Inhibit mode can be set, and the original display file executed to erase the drawing.

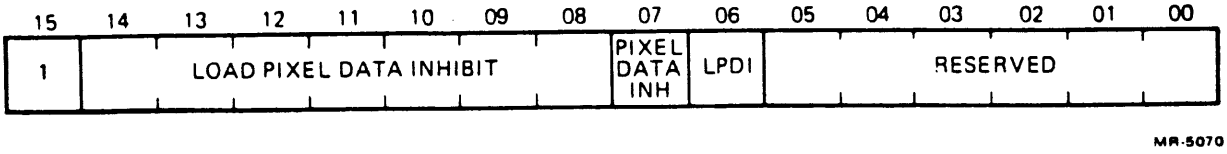


Figure 3-38
LOAD PIXEL DATA INHIBIT Instruction Format

Table 3-35
LOAD PIXEL DATA INHIBIT Instruction Bit Definitions

Bit	Name	Description
15	-	"1" indicates Control word.
14-8, 6	Op-Code	"1111000x0" specifies the LOAD PIXEL DATA INHIBIT instruction.
7	PDI (Pixel Data Inhibit)	"0" clears the internal Pixel Data Inhibit flag, allowing the Graphic Mode instructions to load new pixel data. "1" sets the internal Pixel Data Inhibit flag, inhibiting the Graphic Mode instructions (except Run- Length mode) from loading new pixel data.
5-0	Reserved	Must be written to 0.

3.5.2.14 MARKER NO-OP -

The MARKER instruction is a No-op with ten free (unused) bits that can be used by software to "mark" locations in the display file in order to facilitate manipulation of the file. Figure 3-39 illustrates the instruction format and Table 3-36 describes the bit fields. No operations are performed by this instruction.

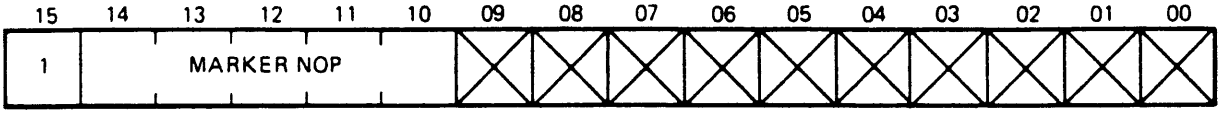


Figure 3-39
MARKER No-Op Instruction Format

Table 3-36
MARKER Instruction Field Definitions

Bit	Name	Definition
15	-	1 indicates Control word.
14-10	OP-CODE	MARKER No-Op Instruction Op-Code.
9-0	Not Used	These bits are not used. They are available for user applications.

3.5.3 Special Instructions

BIT-MAP-0, BIT-MAP-1, and DMA PIXEL READBACK comprise the set of Special instructions. These instructions transfer pixel-by-pixel data between host CPU memory and VSV11/VS11 Image Memory. These instructions are placed in a special class because they deal with data items (packed pixel words and buffer addresses) that cannot use bit 15 of a word to distinguish between data and control information. They operate in a manner similar to the Control instructions in that they do not change the current Graphic Mode of the Display Processor. However, because these instructions cause the Display Program Counter (DPC) to be saved in the PCSAVE register (so that DPC can be used as an address for pixel DMA transfers), they cannot be executed from a display subroutine. Such an attempt would cause a Sequence Error stop to be taken.

Pixel data is handled in two formats, shown in Figure 3-40. The format is selected by bit 9 of the first word of the special instuctions. When bit 9 is zero (0), the four 4-bit pixels per word format is selected. Pixels are packed right-to-left within the word (the first pixel handled is in bits 3-0, the second is in bits 7-4, the third is in bits 11-8 and the last is in bits 15-12). When bit 9 of the instruction word is set (1), two 8-bit pixels per word are expected. The first pixel is in the least-significant (right) byte (bits 7-0) and the second pixel is in the most- significant (left) byte (bits 15-8).

Each of the Special Instructions contains a buffer address pointer, defining the start of the host CPU memory area containing the pixel data to be transferred. This buffer can be in either the Main or Auxiliary display-file segment, as selected by bit 0 of the buffer address parameter word (0 selects the Main segment, 1 selects the Auxiliary segment).

The following paragraphs describe each of the Special instructions in detail.

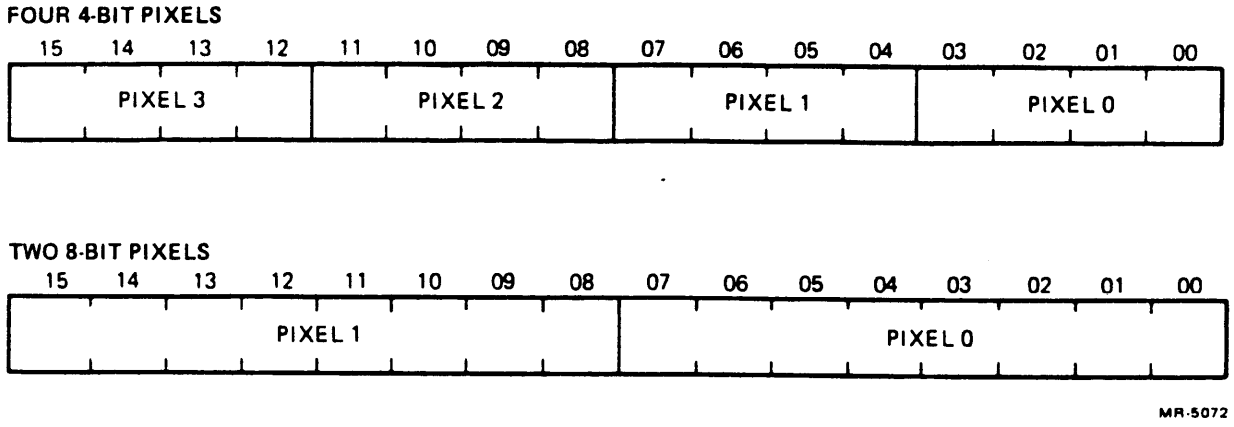


Figure 3-40
BIT-MAP Data Word Formats

3.5.3.1 BIT-MAP 0 -

The BIT-MAP-0 instruction moves a square array of pixel data from host-CPU memory into VSV11/VS11 Image Memory, optionally scaling (expanding) and "smoothing" the array. The source array is retrieved from host memory via a virtual buffer address accompanying the BIT-MAP-0 instruction. The array can be located in either the main or auxiliary display file segment. Arrays of 32 x 32, 64 x 64, 128 x 128 and 256 x 256 pixels are handled. The pixels can be either 4 bits wide, packed four to a 16-bit PDP-11 memory word, or 8 bits wide, packed two to a word. The data word formats are shown in Figure 3-40.

The source array can be moved directly to Image Memory, or can be expanded, with or without smoothing (linear interpolation between pixel intensities), by a factor of 2, 4, or 8. Pixel data is loaded into Image Memory beginning at the current X-Y graphic position, first left to right, then up. Therefore, the source array must be organized with all data for the bottom line first, followed by all data for the second line, etc.

When processing is complete, the X-Y graphic position is located just beyond the top right-hand corner of the resulting display. The graphic mode is not changed by the BIT-MAP-0 instruction, since only one buffer address can accompany the instruction. Operation continues by retrieving the next instruction in the main display file.

The BIT-MAP-0 instruction cannot be executed from a display subroutine (which implies that it cannot be executed from the auxiliary file segment). An attempt to circumvent this restriction results in a SEQUENCE ERROR stop.

Figure 3-41 illustrates the BIT-MAP-0 instruction and Table 3-37 describes each bit in detail.

Figure 3-42 illustrates the results of transferring four pixels from the source array into Image Memory, showing the effects of expansion and smoothing. In the linear smoothing algorithm, calculated intensities of pixels are determined by either two known (source) pixels (if the pixel being calculated is on a horizontal or vertical line between the two known pixels) or four known pixels (if the pixel being calculated is within the square defined by the four known pixels).

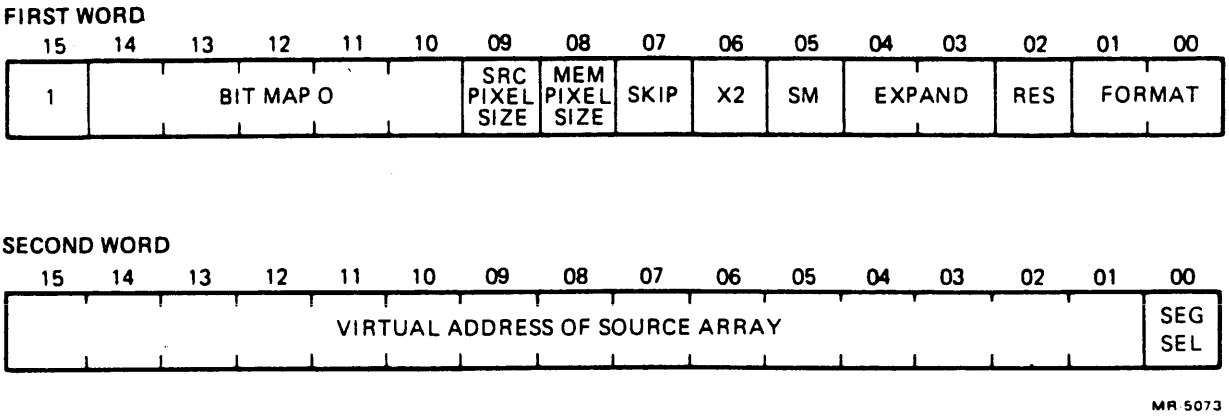


Figure 3-41
BIT-MAP-O Instruction Format

Table 3-37
BIT-MAP-O Instruction Bit Descriptions

	Bit	Name	Description
1st Word	15	-	"1" indicates control word.
	14-10	Op-Code	"01110" indicates BIT-MAP-O Instruction op-code.
	9	SRC PIXEL SIZE (Source Pixel Size)	Indicates how many bits of instensity/color defines a pixel (picture element) from the source array: "0" = 4-bit pixels (4/word) "1" = 8-bit pixels (2/word)
	8	MEM PIXEL SIZE (Memory Pixel Size)	Indicates the pixel color/ intensity resolution of the Image Memory (used during smoothing to round calculated pixel intensities to the proper precision). "0" - 4-bit pixel "1" - 8-bit pixels [Note: Smoothing calculations are carried out to 11-bit precision; rounding occurs only just before a pixel is written and not during intermediate steps of the calculation].
	7	SKIP (Skip Pixels) [M7064 Rev. C or above.]	Setting this bit causes pixels to be written only into alternate Image Memory locations, effectively doubling the size of the image. No pixels are discarded. Rather, the X and Y coordinates are stepped by 2 pixels instead of 1 when data is written. For units with Version 1 microcode (M7064 circuit Rev. B or below), this bit should be set to 0.

(cont'd on next page)

Table 3-37 (cont'd)
BIT-MAP-0 Instruction Bit Descriptions

	Bit	Name	Description
1st Word	6	X2 (Double Expansion)	Setting this bit provides an additional level of expansion (x2). Normally used with Non-Interlaced displays to enable display of all pixels. This bit could roughly be called a "screen resolution" bit, where "0" = full screen of 512 by 512 pixels "1" = full screen of 512 by 256 pixels
	5	SM (Smoothing Enable)	Setting this bit causes an array to be smoothed while it is expanded; [i.e., linear interpolation is performed by the DPU to calculate the intensity of pixels written (from the source array)]. When this bit is 0, intermediate pixels of an expanded array are just duplicates of the known pixels. Smoothing is carried out over the full expansion (bit 6 together with bits 4 and 3).
	4-3	EXPAND (Expan-sion) (Scaling)	Used together with bit 6 to define the factor by which the source array is to be expanded. Expansion options are as follows: (6) (4) (3) Expansion 0 0 0 x1(no expansion) 0 0 1 x2 0 1 0 x4 1 0 0 x2 1 0 1 x4 1 1 0 x8 x 1 1 Reserved (causes Rsv'd OP error if EN RCHK=1; if EN RCHK=0, operates same as x1.

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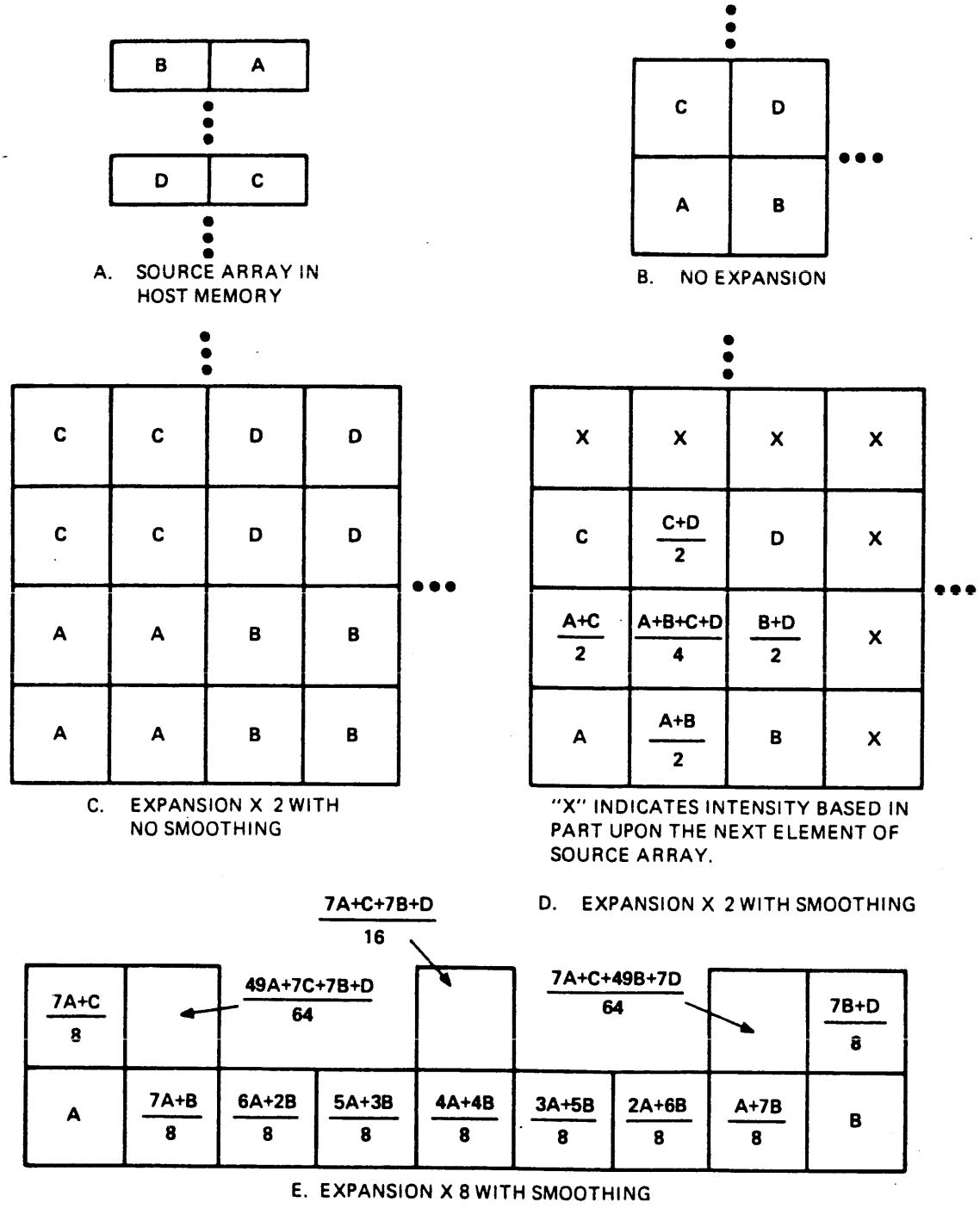
Table 3-37 (cont'd)
BIT-MAP-0 Instruction Bit Descriptions

	Bit	Name	Description
1st Word	2	-	Reserved. If set, causes RSVDOP error stop if EN RCHK=1. Ignored if EN RCHK=0.
	1-0	FMT (Format)	Two-bit code specifying the format of source data array to be acted upon by the DPU: 00 = 32 x 32 pixel array 01 = 64 x 64 pixel array 10 = 128 x 128 pixel array 11 = 256 x 256 pixel array
2nd Word	15-01	Buffer Address	Specifies the virtual address of the start of the source data array.
	0	SEG (Segment Select)	"0" = array is in Main segment "1" = array is in Auxiliary segment.



NOTE:
A, B, C, AND D ARE PIXEL INTENSITIES FROM THE SOURCE ARRAY.

MR-5074

Figure 3-42
BIT-MAP-O Pixel Transfer Examples

3.5.3.2 BIT-MAP-1 -

The BIT-MAP-1 instruction transfers a string of pixels from host memory into sequential horizontal locations in Image Memory (left to right). Up to 512 pixels (one horizontal scan line) can be transferred with one BIT-MAP-1 instruction. Both of the data formats shown in Figure 3-40 are handled. Pixel transfer into Image Memory includes and proceeds from the current graphic position.

As shown in Figure 3-43 and Table 3-38, BIT-MAP-1 is a two-word instruction. The first word specifies BIT-MAP-1 with the Op-Code in bits 14-10. Bit 9 specifies the format of the source data. Bits 8-0 specify the number of pixels to be transferred; a zero in this field specifies that 512 pixels are to be transferred. The second word specifies the starting address in host memory of the source pixel string: bits 15-1 specify the virtual word address and bit 0 selects the display file segment.

After each pixel is transferred, the X position is stepped by one pixel (by 2 in the 1024-point-resolution coordinate scheme). Therefore, the final X coordinate (in DXR) is equal to the starting X coordinate plus twice the pixel count. Note that the Y position is never modified by the BIT-MAP-1 instruction.

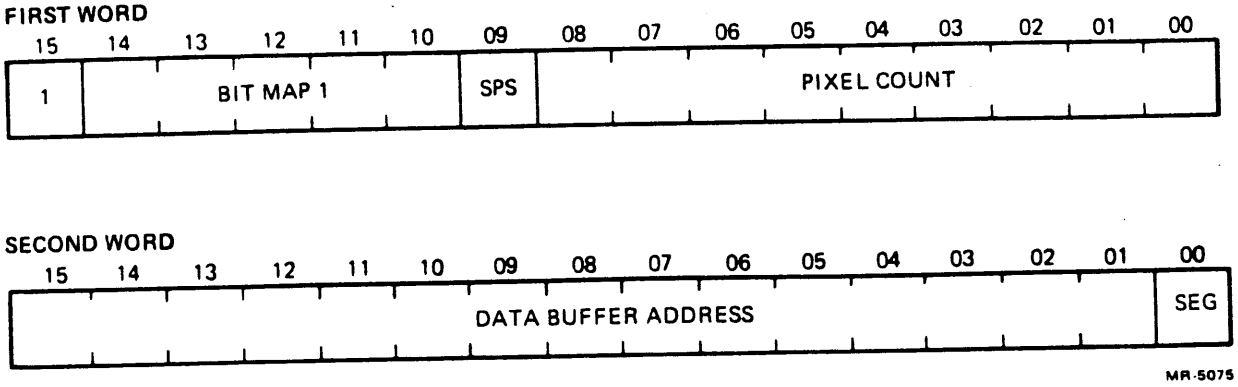


Figure 3-43
BIT-MAP-1 Instruction Format

Table 3-38
BIT-MAP-1 Instruction Field Definitions

	Bit	Name	Description
1st Word	15	-	"1" indicates Control word.
	14-10	Op-Code	"01111" specifies BIT-MAP 1 instruction.
	9	SPS (Source Pixel Size)	Indicates how many bits of intensity/color defines a pixel (picture element): "0" = 4 bit pixels (4/word) "1" = 8 bit pixels (2/word)
	8-0	PIXEL COUNT	Specifies the number of pixels which will be written into Image Memory. (A 0 in this field specifies a count of 1000 octal [512 pixels].
2nd Word	15-1	Data Buffer Address	Specifies the virtual address of the source buffer. Contains a 15 bit number which, when added to the shifted "Relocate Register" of the selected segment, gives an 18 bit, LSI-11 Bus address specifying the start location of pixel data.
	0	SEG (Segment Select)	SEG=0 specifies that BIT-MAP source data is in the Main display-file segment; SEG=1 specifies that data is in the auxiliary segment.

3.5.3.3 DMA Pixel Readback -

The DMA Pixel Readback instruction, illustrated in Figure 3-44 and described in Table 3-39, causes a rectangular area of Image Memory to be read into host CPU memory in Bit-Map data format. Reading proceeds line by line, either bottom-to-top or top-to-bottom. Either of the Bit-Map data formats shown in Figure 3-40 can be selected.

As shown in Figure 3-44, the instruction has two forms: a START configuration and a RESTART configuration. The START configuration is a five-word instruction used to initiate the reading of a rectangular array of pixels, starting at the current X-Y graphic position. The first word of the instruction specifies the DMA Pixel Readback op-code in bits 14-10. Bit 9 selects the format to be used for storing the pixel data in host memory. Bits 7 and 6 specify the action to be taken with respect to the Y position when a read of one horizontal line of the source rectangle is complete; Y can be stepped either up or down by one or two pixels. Bits 2 and 1 select a mask to be applied to the pixel data received from Image Memory so that unused data bits can be cleared. Bit 0 of the first instruction word determines whether the instruction is a START (bit 0 = 0) or RESTART (bit 0 = 1).

In the START configuration, the second and third instruction words specify the width (in number of pixels) and height (number of lines) of the rectangular area, respectively. The fourth word specifies the maximum number of 16-bit words to be transferred into host memory. The fifth instruction word contains the virtual address of the buffer in host memory to receive pixel data; bit 0 selects the segment.

On a START, the instruction word is stored in DSR and the current graphic X position and the width and height parameters are saved in internal Display Processor registers. Transfer of pixels from Image Memory to host memory then proceeds until (1) the number of pixels specified by the width and height parameters have been transferred, or (2) the word count expires (decrements to 0). In the first case, display processing stops with the original instruction (first word) in the DSR register, with bit 0 clear (0). In the latter case, processing stops with bit 0 of DSR set (1). In both cases, the Display Program Counter (DPC) contains the address of the word following the last data word stored. [With Version 2 microcode in the DPU, M7064 module Rev. C or above, if bit 5 of the first instruction word is set, the display program will continue with the instruction following the DMA Pixel Readback instruction if all pixels specified have been read before the Word Count expires.]

The RESTART instruction is a 3-word instruction used to continue the reading of pixels within the same rectangle established by the START instruction, using the stored width and height parameters. Reading proceeds from the current position. The original X position, saved by the START, and the count of the

number of pixels remaining in the rectangle, remain intact. Because the RESTART instruction depends upon several parameters stored internally, no other type of display processing must be performed between the time a DMA Readback stops and the time a RESTART is issued. Furthermore, the Resume operation (writing a 1 into bit 0 of the DPC) cannot be used after a DMA Readback, since DPC contains a buffer address and not the address of the location following the DMA Readback.

The RESTART instruction allows a large rectangular area of the screen to be handled in blocks of data supported by other devices, such as disk or magtape. In such cases, the Word Count parameter would be set to the size of disk or magtape block to be handled, using as many RESTARTS as required to read all of the required pixels.

The "edge detection" logic in the image memories does not operate during pixel readback. Therefore, reading is performed at coordinates modulo the visible screen size (wraparound occurs). Also, only image memories that are in Write-Only or Read/Write mode can be read.

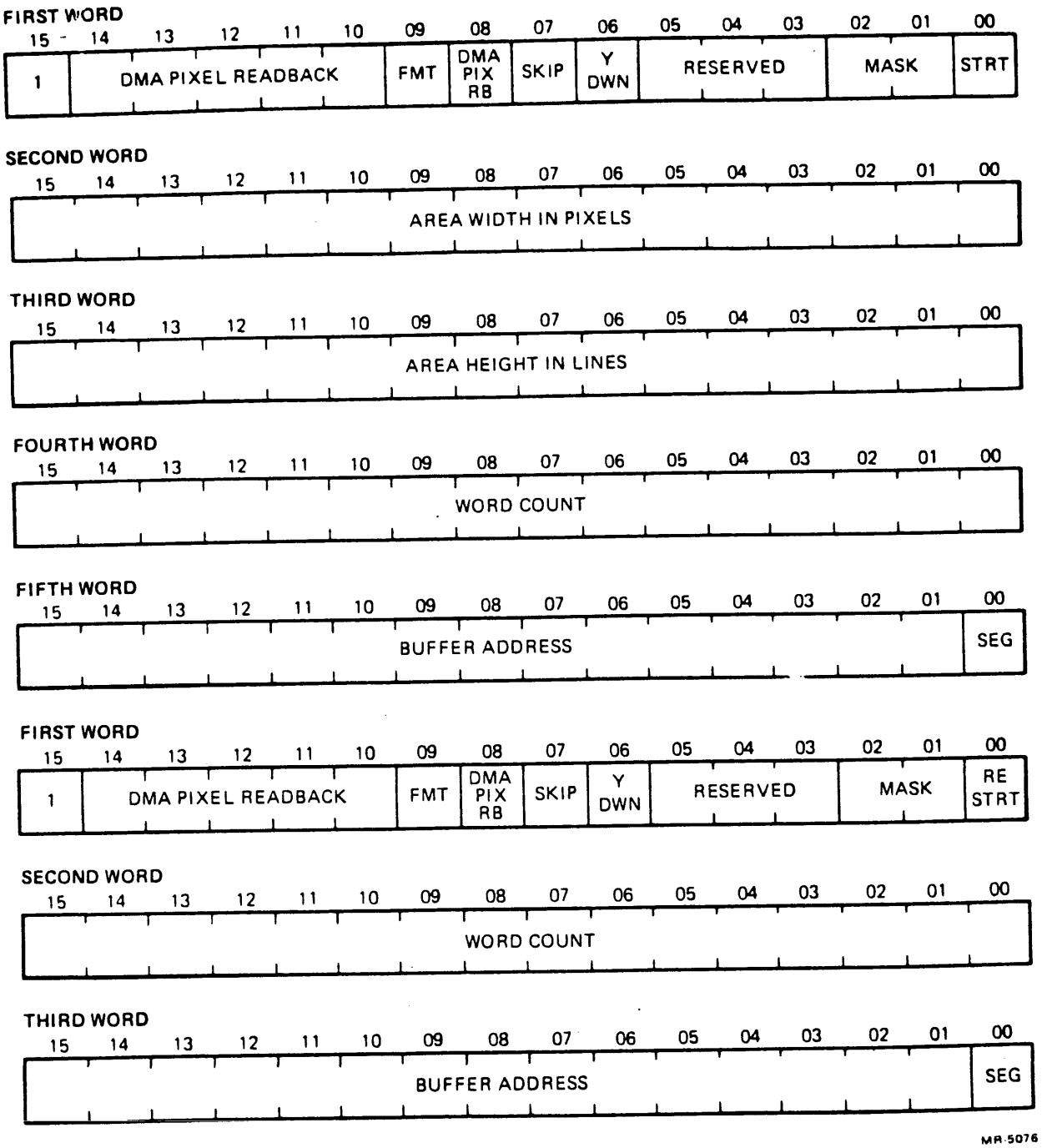


Figure 3-44
DMA Pixel Readback Instruction Format

Table 3-39
DMA Pixel Readback Instruction Bit Definitions

	Bit	Name	Description
1st Word	15	-	1 indicates Control word.
	14-10, 8	Op-Code	DMA Pixel Readback instruction Op-Code.
	9	FMT (Format)	"0" specifies data to be stored four 4-bit pixels per 16- bit word. "1" specifies data to be stored two 8-bit pixels per 16- bit word.
	7	SKIP	"0" specifies that the Y position steps by 2 (1 pixel) upon completion of horizontal line. "1" specifies that the Y position steps by 4 (2 pixels) upon completion of horizontal line (used for reading Non-Interlaced memory).
	6	Y DOWN	"0" specifies that the Y position is to be stepped up (incremented) after completion of a horizontal line. "1" specifies that the Y position is to be stepped down (decremented) after completion of a horizontal line.
	5	CONT (Continue) [M7064 Rev. C or above.]	If 0, processing always stops if either the Word Count expires or the entire array has been read. If 1, processing will stop only if the entire array is not read before the Word Count expires. [For M7064 modules Rev. B or below, this bit should always be coded as 0.]

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Table 3-39 (cont'd)
DMA Pixel Readback Instruction Bit Definitions

	Bit	Name	Description
1st Word	4-3	-	Reserved. Must always be written to 0.
	2-1	MASK	Specifies a mask to be ANDed with image memory data before it is packed into words, allowing unused memory bus bits to be masked off. The mask is selected as follows: 2:1 — No. of Pixel Bits — DBUS Mask Value 0 0 — 2 — 1400 0 1 — 4 — 1700 1 0 — 6 — 1760 1 1 — 8 — 1774 NOTE: The masks for 6-and 8- bit pixels should not be issued when the FORMAT bit is 0.
	0	RESTART	"0" specifies a DMA Readback START, indicating a 5-word instruction. "1" specifies a DMA Readback RESTART, indicating a 3-word instruction. The entire first instruction word must match the current contents of the DSR register or else Sequence Error stop is taken.
2nd Word	15-0	WIDTH	Specifies the width, in number of pixels, of the image memory area to be read. Values of 1-512 produce reasonable results. Values greater than 512 will cause some pixels to be read more than once, since wraparound of the visible area occurs.

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Table 3-39 (cont'd)
DMA Pixel Readback Instruction Bit Definitions

	Bit	Name	Description
3rd Word	15-0	HEIGHT	Specifies the height, in number of pixels, of the Image Memory area to be read. Values of 1-512 produce reasonable results. Values greater than 512 will cause some lines to be read more than once, since wraparound of the visible area occurs.
4th Word	15	-	Reserved. Should always be coded as 0.
	14-0	WORD COUNT	This field specifies the number of 16-bit words to be written into host CPU memory; ie., the Word Count specifies the size of the destination buffer.
5th Word	15-1	BUFFER ADDRESS	Specifies the virtual address of the area in host CPU memory where the pixel data words are to be deposited.
	0	SEG (Segment Select)	Specifies the display file segment containing the destination buffer: "0" = Buffer is in Main Segment "1" = Buffer is in Auxiliary Segment

3.6 HOST MEMORY DISPLAY FILE MAKE-UP

The display file can be defined as the sum total of all instructions (Control, Graphic and Data) stored in the CPU memory to display an image on the system monitor. These instructions are placed in consecutive memory locations and are automatically fetched by the VSV11/VS11 Display Processor through DMA requests.

The display file make-up is the same for LSI-11 (VSV11 systems) or PDP-11 (VS11 systems) memories. In structuring of a display file, the usual sequence of instructions is:

1. Control Instructions - these instructions include Set Character Base, JUMP, DNOP/POP, and the Load Status instructions. Generally, the VSV11/VS11 system is conditioned (set the Display Processor to stop and interrupt, set-up the memory Read/Write mode and Switch bit, etc.) with these instructions.

2. Graphic Mode Instructions - these instructions set the graphic mode (Character mode, Vector mode, Graph/Histogram mode, etc.) and set the intensity/color of the displayed pixel information.

3. Graphic Data Instructions - these instructions convey the data to be displayed in a particular graphic mode.

An example of a short, simple display file is as follows:

Notation	Octal Machine Code	Instruction
WRT CH0	176030	Load Status Register C (set memory 0 to Write mode, enable Switch)
APNT	114000	Point Mode (Absolute)
0, 0	0, 0	Point Mode Data
LVEC+ PIX	113777	Long Vector Mode, Set all Intensity bits
I,511	41776	Vector Mode Data 1st Word
0	0	Vector Mode Data 2nd Word
I,0	40000	Vector Mode Data 1st Word
479	1676	Vector Mode Data 2nd Word
I,-511	61776	Vector Mode Data 1st Word
0		0 Vector Mode Data 2nd Word
I,0	40000	Vector Mode Data 1st Word

479	21676	Vector Mode Data 2nd Word
SWITCH	170200	Load Status Register A
STOP	172000	Load Status Register A

This program will produce an image of a rectangle on the system monitor. The first instruction (176030) selects Image Memory channel zero, selects the Write mode for the Image Memory, and sets the Switch Enable bit fot the memory. Instruction 114000 sets the Absolute Point mode. The point mode instruction places the system monitor pixel position within the viewable area of the CRT, in this example the lower left corner as specified by the point mode data word (0,0). Because the point mode data word contains a zero in bit 14 (Intensity), the pixel position will not be visible on the system monitor.

Next, the Long Vector mode (113777) is used to produce the vectors required to draw a rectangle. The 113777 instruction sets the long vector mode, enables the specified intensity, and sets the pixel intensity (maximum in this example). Long Vector mode is followed by four pairs (first and second words) of data words for the Long Vector mode. These data words specify the X and Y coordinates of vectors which produce the displayed rectangle. The x coordinate (contained in the first data word) is always the first to be specified; this is followed by the Y coordinate (second data word). The notation indicates that the sides of the rectangle are 512 units (0-479) and 480 units (0-479) in length. This is the maximum size of a rectangle that can be displayed on the VSV11/VS11 system monitor at 60 Hz. Because the coordinate system used in VSV11/VS11 system is formatted for a maximum display resolution of 1024 units, the vector data words for the 479 X and Y coordinates (41776, 1676, 61776, 21676) are written specifying coordinates of 1024. The VSV11/VS11 Display Processor divides 1024 by two to produce the 512 (0-511) coordinates.

The first Load Status A instruction (170200) sets the Switch bit which was previously enabled with the Load Status C instruction. When the Load Status A instruction is processed, the Image Memory automatically switches from the Write mode (Display Processor writing to the memory) to the Read mode (Image Memory contents read to system monitor). This allows the contents of the Image Memory to be displayed on the system monitor.

The last instruction is a STOP instruction (172000). Stop is programmed with a Load Status A instruction by setting bit 10 of the instruction. Since only bit 10 has been set, the display will stop without generating an interrupt to the CPU.

The only things not specified in the example program are the memory locations where the program is stored. Sequential memory locations are assigned to the program instructions starting with the first instruction (176030). Once the program has been assigned locations, the address of the first location is transferred to the VSV11/VS11 DPC to start execution.

CHAPTER 4

M7064 DISPLAY PROCESSOR TECHNICAL DESCRIPTION

4.1 INTRODUCTION

The M7064 is a quad-height module used in the VSV11/VS11 system as the Display Processor (abbreviated DP). It resides on the host CPU's LSI-11 Bus (implemented with a DW11 UNIBUS to LSI-11 Bus Converter for UNIBUS systems) and functions as the interface between the host CPU, the memory and the other VSV11 components (Image Memories, Sync Generator/Cursor Control modules).

The Display Processor has four addressable registers in the I/O address page of the LSI-11 Bus. This allows the host CPU to have direct "device driver" level control over the VSV11/VS11 system. User-level control, for displays, is provided by instructions from a display file located in host CPU memory. These display file instructions are fetched automatically by the DP via Direct Memory Access (DMA) bus requests and actually write the data into the Image Memory to "draw" pictures on the screen. A ROM controlled, microprogrammed microprocessor within the DP interprets the display instructions to produce short vectors, long vectors, graphplots, points and "bit map" images on the system monitor. Display instructions also control the Image Memories and the Sync Generator/Cursor Control modules. The display instruction set, as well as I/O register programming, is covered in Chapter 3. The following paragraphs discuss the M7064 hardware structure, its operation and interfacing to the other system components, and some of the microprogrammed sequences implemented. It is assumed that the reader is familiar with the theory of operation of the LSI-11 Bus.

4.2 GENERAL DESCRIPTION

Figure 4-1 is a basic block diagram of the Display Processor. There are four major sections within the DP:

1. LSI-11 Bus Interface: Consists of the standard LSI-11 family of bus interface integrated circuits for handling data, interrupt requests, and DMA requests.

2. Bit-Slice Microprocessor Data Paths: The Microprocessor Data Path is constructed around four 4-bit slice 2901A integrated circuits. The circuits provide 16-bit data manipulation for arithmetic, logical functions, and storage (seventeen 16-bit registers). Augmenting the basic data path is a Scratchpad RAM that provides 16 words by 16 bits of additional storage.

3. Data Bus (DBUS) Interface: Consists of drivers and receivers for the flat-cable bus connecting the DP to the Image Memories and Sync Generators. Using the DBUS, the DP transmits X and Y coordinates and pixel data to the Image Memories. Control information is also transmitted into the Memory and Sync (joystick and cursor) control registers. The DP receives information from the Image Memory and Sync modules as pixel data from a specified memory location and cursor coordinates from the currently active sync module. The DBUS Interface contains a control register that allows the microprogram to access a particular Sync or Memory register.

4. Control ROM and Sequencer: All the operations of the DP are under the control of the microprogram stored in the Control ROM (Read-Only Memory). The microwords stored in the ROM are 64 bits wide and contain the field bits which control the other elements of the DP, such as the LSI-11 Bus Interface, Microprocessor Data Path, and DBUS Interface. Associated with the ROM is a Sequencer circuit that supplies the address of the next microword to be executed. The Sequencer is under control of the fields within the microword and can be programmed to execute sequential microwords, jumps, subroutine calls, and subroutine returns. The output of the ROM does not go directly to the other DP elements. The ROM output is clocked into a Pipeline Register, which in turn controls the other DP elements. This pipelined structure maximizes performance by allowing one microword to be executed while the next one is being fetched.

Within the DP, the major elements communicate using two internal buses: the Data/Address Lines (DAL Bus), corresponding to the BDAL lines of the LSI-11 Bus, and the SRC Bus which "sources" the data used by the 2901A elements. Data being transmitted via the LSI-11 Bus or DBUS is produced in the 2901A and is gated onto the DAL bus to the respective element. The DAL bus can also carry the data received from the LSI-11 Bus BDAL lines. This data is normally stored in the Scratchpad RAM for subsequent transmission (over the SRC bus) to the 2901As. The SRC bus carries data from the Scratchpad RAM, the DBUS receivers, and the EMIT field of the microword. The EMIT field allows 16-bit data constants to be received by the 2901As for use as count values, masks, or microprogram addresses. The SRC bus is also used to provide a calculated microprogram address for the 2909 Sequencer. This allows great flexibility in the microprogram flow.

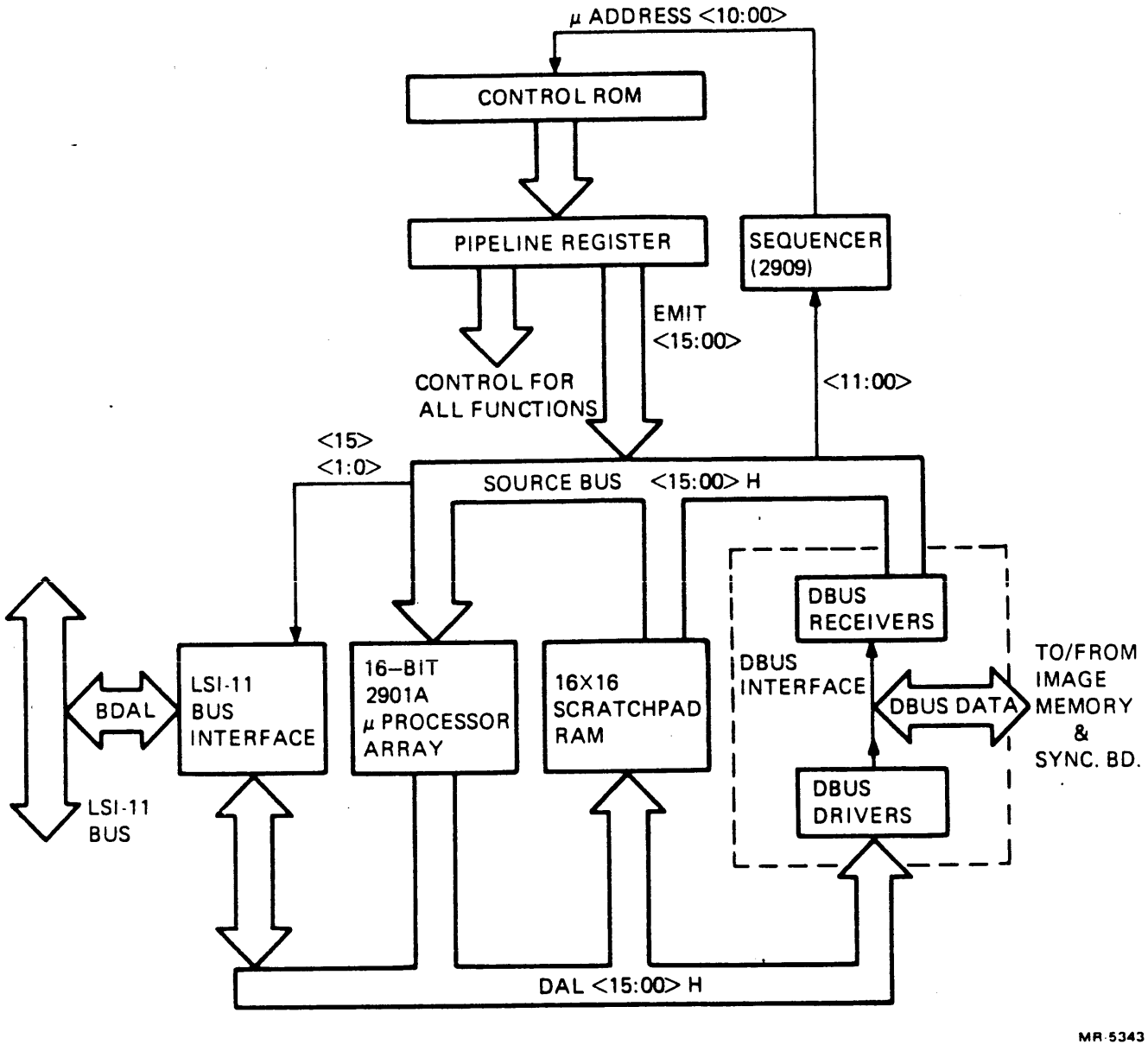


Figure 4-1
Display Processor Basic Block Diagram

4.3 FUNCTIONAL DESCRIPTION

The following paragraphs contain a general functional description of the major hardware sections within the DP. Each section is expanded and discussed in terms of its detailed block diagram and the specific functions it performs. It must be kept in mind that all sections of the Display Processor must function together under direction of the microprogram in order to implement the

overall DP functionality. None of the sections functions individually. Therefore, where necessary the section's interaction with the others is included in the discussion. The simplified microprogram "overview" flowchart and discussion in Paragraph 4.4 can be referenced when microprogram control of the various elements is discussed.

4.3.1 LSI-11 Bus Interface

The LSI-11 Bus Interface section provides the interface between the LSI-11 Bus, the host CPU and its memory, and the entire VSV11 display system. Under control of the microprogram in the DP Control ROM, the interface makes LSI-11 Bus requests for interrupts and DMA transfers. It also responds to programmed I/O accesses to addresses within its device register range, and handles the data transferred between the host CPU and its memory, and the internal DP registers.

Data transfers between the host CPU and the DP are termed programmed-I/O transfers. That is, the host CPU can read and write the DP Display Program Counter (DPC, bus address 77xxx0), the Display Status Register (DSR, bus address 77xxx2), and the X and Y Status Registers (DXR and DYR, bus addresses 77xxx4 and 77xxx6, respectively). However, unlike many LSI-11 Bus devices, these registers are not implemented with discrete hardware interfaced directly to the LSI-11 Bus. Rather these registers are "soft" registers, with actual data storage implemented within the general structure of the microprocessor data paths and functionality totally defined by the microprogram itself. The LSI-11 Bus Interface merely provides the path between these internal registers and the LSI-11 Bus.

Figure 4-2 is a detailed block diagram of the LSI-11 Bus interface. The Transceivers/Device Address Selector/Vector Address Generator (DC005), the Interrupt Logic (DC003), the Protocol Logic (DC004), and the DMA Control logic (DC010) are all standard LSI-11-Family interface integrated circuits. These are described in the Microcomputer Interfaces Handbook.

Most of the control signals for the LSI-11 Bus interface are supplied from the QBUS Control Register. These are loaded from the general-purpose EMIT field of the microword. The QBUS Control Register contains bits to enable the drivers onto the LSI-11 Bus BDAL lines, request interrupts and DMA mastership, and provide signals required by LSI-11 Bus protocol rules for DMA data transactions. Also provided by the microword are three Strobe pulses (to handle the STALL flip-flop and initializing of the DC010) and an enable for gating the received LSI-11 BDAL lines onto the internal DAL bus.

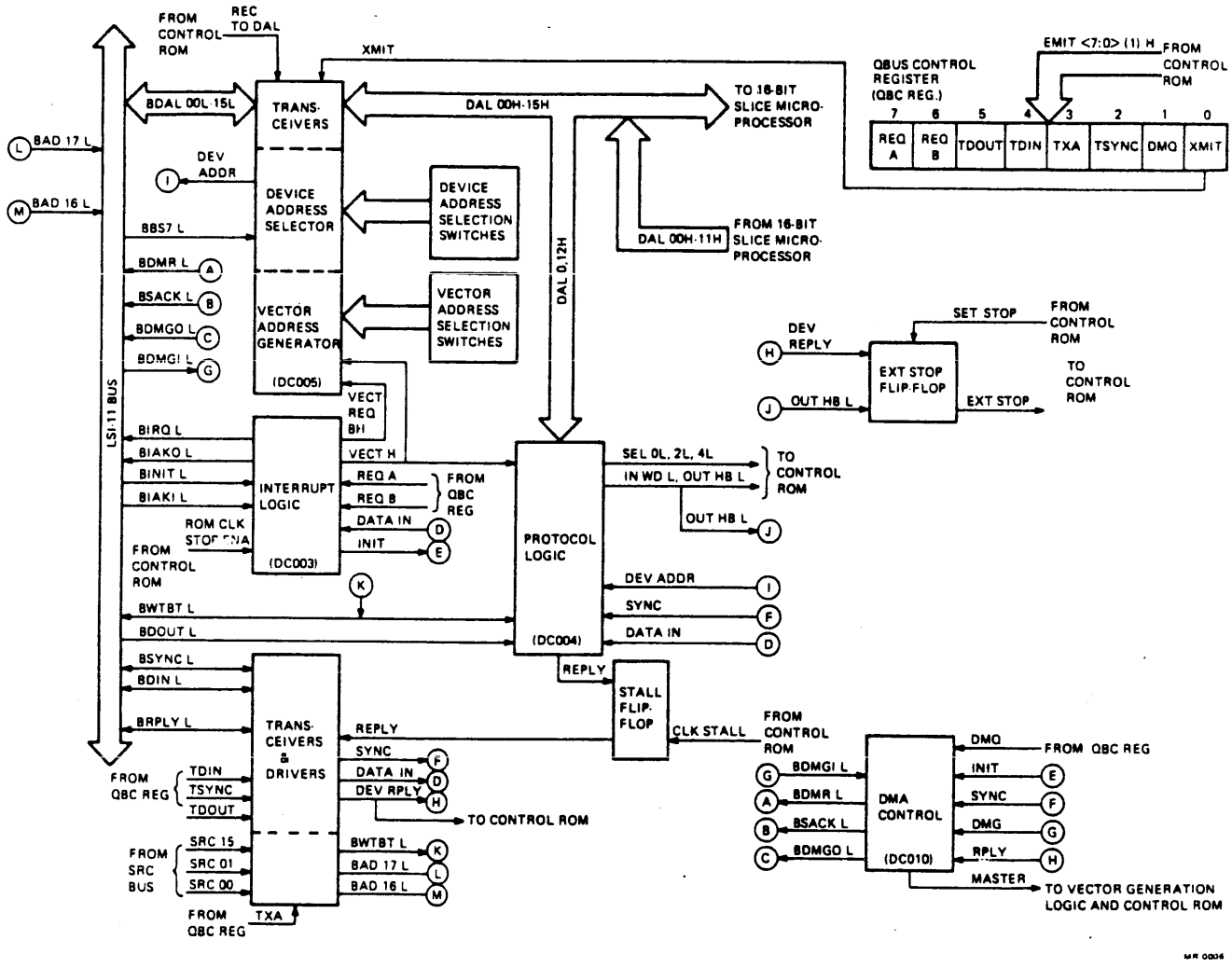


Figure 4-2
LSI-11 Bus Interface Block Diagram

4.3.1.1 Programmed-I/O Transfers -

As mentioned previously, the Display Processor implements four "soft" addressable device registers on the LSI-11 Bus. These registers (DPC, DSR, DXR, and DYR) are found at the general addresses 17xxx0 through 17xxx6 in the LSI-11 Bus I/O page. The location of this block can be changed via the Device Address Selection switches connected to the DC005 Transceiver/Decoder circuits.

Access to the registers is meaningful only when the Display Processor is in the Idle state, since it is the microprogram that must implement the actual register response. In the Idle state, the DP microprogram is not Busy fetching, interpreting and executing display file instructions. When the DP is Busy, the microprogram enables the bus interface to produce a Reply response on the LSI-11 Bus in response to an attempted access, but no data is read or written.

The Idle state is entered initially after the Display Processor is powered up. During power-up, or a RESET instruction executed in the host CPU, BINIT L is present on the LSI-11 Bus and is received by the DP (DC003 circuit).

The BINIT L (initialize) signal forces the microprogram Sequencer to set the microprogram Control ROM to address zero. When BINIT L negates, the microprogram begins the execution of a startup routine at address zero. The startup routine loads most internal registers in the 2901A and Scratchpad RAM to a known state, usually zero, performs a self-test on DBUS data and status lines, and self-tests some backplane Video Bus status signals. It also sets all Image Memories to the Write-Only mode, clears them to zero, and clears the Switch, Match, and Crosshair enable bits in all Sync module Joystick Status registers. Following the startup sequence, the microprogram proceeds to the Idle-Stop sequence and prepares for entry into the Idle state by clearing the "STALL" flip-flop. After STALL is cleared, causing all responses for register accesses to be blocked until handled by the microprogram, the microprogram proceeds to the Idle Loop and awaits a register access by the host CPU.

Assuming that the host CPU is going to write (DATO) to the DP Display Program Counter (DPC) register, the CPU places the DPC address (17xxx0) onto the LSI-11 Bus BDAL lines, asserts BBS7 (Bank Select 7, specifying the I/O page), and asserts BDOUT L and BSYNC L. The DP receives and decodes the DPC address in the DC005 circuits. (Device address decoding is set up by the Device Address Selection switches as explained in Chapter 2.) If the incoming address (bits 15--03) matches the address set up in the Device Address Selection switches, the Device Address Selector produces the DEV ADDR signal. DEV ADDR is strobed into the Protocol logic by SYNC, which in turn produces REPLY. If the DP is Idle, the STALL flip-flop will be clear and REPLY will not be returned to the LSI-11 Bus. The strobing in of DEV ADDR enables the Protocol logic to decode bits DAL 00, 01, and 02 of the address. In turn, the Protocol logic produces SEL 0 which causes

the Control ROM to select the DP Display Program Counter for access. Note that in the Idle Loop, the microprogram is continually gating the LSI-11 BDAL lines onto the internal DAL bus to allow the Protocol logic to properly decode the address.

The host CPU now removes the register address from the LSI-11 Bus and asserts the data to be written into DPC (which is implemented as one of the registers in the 2901A bit-slice array). The microprogram enables this data onto the internal DAL bus and then loads it into the MBUF register in the Scratchpad RAM (Figure 4-1). From MBUF, the data is gated onto the internal SRC bus and is subsequently loaded into the Q-Register of the 2901A, a temporary holding register.

After the data is taken, the microprogram sets the STALL flip-flop to allow the REPLY signal to pass to the LSI-11 Bus as BRPLY L. When the CPU receives BRPLY, it removes the data from the BDAL lines and negates BDOUT. This causes REPLY and hence BRPLY to be negated. When BRPLY negates, the CPU negates BSYNC to complete the DATO cycle.

Because the DPC register was written, the microprogram enters its WRTDPC routine to begin display file processing. The STALL flip-flop is allowed to remain set so that subsequent register accesses will elicit a response from the DP. The DP is now considered to be in the Busy state and will not allow the internal registers to be read or written. Bit 00 of the data in the Q-Register is tested. If it is a zero, a Start sequence is specified by the CPU, so the microprogram transfers the contents of the Q-Register to the internal DPC register and establishes a new display-file starting address. If bit 00 of the Q-Register is a one, a Resume sequence is indicated; the internal DPC register remains intact and display-file processing continues at that address.

A DATI (Data-In) cycle occurs when the host CPU reads one of the device register locations (DPC, DSR, DXR, or DYR). Assuming the Display Program Counter (DPC) is to be read, the host CPU places the address of the DPC on the BDAL lines, asserts BBS7, and asserts BSYNC L. The Device Address Selector (DC005) compares the incoming address to the device address selected by the Device Address Selection switches. If the addresses match, the Device Address Selector produces a high DEV ADDR to enable the Protocol logic. SYNC strobes DEV ADDR into the Protocol logic. The Protocol logic now decodes DAL bits 00, 01, and 02 to determine the register selected. For the DPC, the decode of DAL 00, 01, and 02 causes the Protocol logic to enable SEL 0, which the microprogram tests to select the DPC. The host CPU now removes the DPC address from the BDAL lines and asserts BDIN. BDIN enables DATA IN and causes the Protocol logic to produce IN WD. (The state of IN WD is tested by the ROM program to determine DP operations.) The DP then places the contents of the DPC on the BDAL lines (via the internal DAL bus) and asserts BRPLY by setting STALL. When the host CPU accepts the DPC data it negates BDIN. This is followed by the DP negating BREPLY (by clearing STALL), thus completing the DATI bus cycle.

During the I/O transfer examples presented, only the Display Program Counter was discussed. The process of writing or reading the DSR, DXR or DYR registers is similar to that described for the DPC. However, the Protocol logic enables different SEL outputs for the DSR, DXR or DYR registers. SEL 02 results from decoding the DSR address (17xxx2); SEL 04 L is for the DXR register (17xxx4), and a negated condition of SEL 0, SEL 2 and SEL 4 is for the DYR register (17xxx6).

Also, the DP is a word machine. That is, all transfers to/from the DP are word transfers with even-numbered byte addresses. If the DP receives a DATA-OUT-BYTE write cycle, a full word will be written.

All address and data transfers pass though the DP's Transceiver circuits (DC005). The Transceivers are enabled to gate LSI-11 Bus address/data information onto the internal DAL bus (DAL <15:00> H) when the REC TO DAL H signal from the microprogram ROM is high. When the TXMIT bit in the QBUS Control Register (loaded from the microword EMIT field) is set, it enables the internal DAL address/data information (produced by the 2901A elements) to be gated onto the LSI-11 Bus BDAL lines. When the REC TO DAL signal is low, the Transceivers cannot pass LSI-11 Bus information onto the internal DAL bus, allowing that bus to be used for transferring data from the 2901As to the Scratchpad RAM and/or DBUS interface. When the microprogram is in its Idle loop, it continually asserts REC TO DAL to allow LSI-11 Bus address information to pass onto the internal DAL bus, since DAL bits 02-00 are used by the Protocol circuit to decode the specific register address. When the microprogram is in the Busy state, it allows the STALL flip-flop to remain set so that the DP can still respond to the device address on the LSI-11 Bus (i.e., issue BREPLY). This prevents bus "time-out" errors, but the display registers will appear to have all zeros (since DAL will not be gated to BDAL).

4.3.1.2 DMA (Direct Memory Access) Transfers -

The DP performs NPR (Non-Processor) requests to become master of the LSI-11 Bus and then fetch display instructions from the host CPU memory display file. The DP can also write into host CPU memory, such as for storing pixel data from the Image Memory.

The microprogram contains a FETCH subroutine to retrieve data from the host memory, and a STORE subroutine to deposit data. Both routines use the contents of the DPC register as the "virtual" memory address to be accessed. This virtual address is converted into a physical memory address by addition of a relocation value. The addition occurs in the 2901A circuits. Both subroutines call a common routine to perform the address relocation and request bus mastership. A common cycle completion sequence is also used.

Assuming that the DP microprogram is to retrieve (read) data from

host memory, it calls the FETCH subroutine. In FETCH, the DPC is tested to assure that it is within the allowable range. If it is not, processing stops and the DP returns to the Idle state with a Memory Protection error. Assuming the virtual address in DPC is valid, the microprogram requests NPR mastership by setting the DMA REQ bit in the QBUS Control Register. This signal is applied to the DMA Control circuit (DC010), which in turn asserts BDMR L (DMA Request) on the LSI-11 Bus. Meanwhile, the microprogram calculates the physical 18-bit address by adding the current relocation value to DPC. Bits 15-00 of the physical address are stored in the 2901A Q-Register, and bits 17 and 16 of the physical address are stored in the MBUF register in the Scratchpad RAM (Figure 4-1). The microprogram then waits for bus mastership. The host CPU grants bus mastership to the DP by negating BSYNC and BREPLY from the previous bus cycle and asserting BDMGI L (DMA Grant In). When the DC010 sees BDMGI asserted and BSYNC and BRPLY negated, it asserts BSACK (Selection Acknowledge) and MASTER and negates BDMR. The microprogram, having been waiting for the DC010 to issue the MASTER signal, can now proceed with the DATI transfer. First, the microprogram gates the Q-Register onto the internal DAL bus and the MBUF scratchpad register onto the SRC bus. Then it sets the TXMIT and XA TO BAD bits in the QBUS Control Register. This causes the 18-bit physical address to be asserted onto the LSI-11 Bus (bits 15-00 via the DAL bus, and bits 17-16 via the SRC bus). Next, after waiting one microinstruction time (160 nS) to allow for address deskew, the microprogram sets the TSYNC (Transmit SYNC) bit in the QBUS Control Register, causing BSYNC L to be asserted on the LSI-11 Bus. The addressed memory uses the BSYNC assertion to strobe in the address. After the next instruction time, the TXMIT and XA TO BAD bits in QBUS Control are cleared, and the TDIN (Transmit DATA-IN) bit is set. This causes BDIN L to be asserted on the LSI-11 Bus, commanding the addressed memory to read its data and place it on the LSI-11 Bus BDAL lines. The microprogram waits in a loop for BRPLY indicating that the desired data is available. When BRPLY is received, the microprogram exits the loop, asserts REC TO DAL to gate the BDAL data onto the internal DAL bus, and then stores this data in the MBUF Scratchpad register. TDIN is then cleared, negating BDIN, causing the memory to drop the data and BRPLY. Finally, when the microprogram receives negation of BRPLY, it clears the QBUS Control Register (negating BSYNC) to end the cycle. Upon return from the FETCH subroutine, the DPC is incremented by 2 to point to the next location in the display file. The fetched data is copied from the MBUF Scratchpad register, over the SRC bus, into the 2901A Q-Register.

The DATO (Data-Out) transaction performed by the STORE subroutine proceeds similarly to the DATA, except that in place of asserting TDIN, the TDOUT signal is sent, along with the data to be written into host memory.

4.3.1.3 Interrupt Generation -

Four program interrupts to the host CPU can be generated by the DP. These are designated as STOP, CURSOR MATCH, ERROR, and JOYSTICK SWITCH. The vector addresses for these interrupts are in sequential order within a block of eight memory locations. The address of the block is selected by switches on the Display Processor module, as described in Chapter 2. For example, if the switches are configured to start the address block at 320 (octal), the following assignments result:

Interrupt	New PC	New PSW
STOP	320	322
CURSOR MATCH	324	326
ERROR	330	332
JOYSTICK SWITCH	334	336

Interrupts are requested by the microprogram in response to various conditions arising during execution of the display file. In addition, the JOYSTICK SWITCH interrupt can be requested while the DP is Idle. The microprogram initiates the request by setting one of two bits in the QBUS Control Regi ter, depending upon the type of interrupt.

The interrupt sequence is generated by the DC003 Interrupt Control circuit (Figure 4-2). The DC003 contains two sections, A and B. The STOP and CURSOR MATCH interrupts are requested through section A via the RQSTA bit in the QBUS Control Register. The ERROR and JOYSTICK SWITCH interrupts are requested through section B via the RQSTB bit in the QBUS Control Register. During an interrupt sequence, the VECTOR H output of the DC003 goes high and applies the Vector Selection Switches to the DC005 Transceivers, causing the basic vector address to be transmitted onto the BDAL <10:04> lines of the LSI-11 Bus. In addition, if section B of the DC003 is the active section (ERROR or JOYSTICK SWITCH interrupt) the VEC RQSTB H signal is active to cause BDAL 03 to be asserted, effectively adding 10 (octal) to the basic address. Further, the microprogram asserts DAL 02 when the JOYSTICK SWITCH and CURSOR MATCH vectors are to be produced (324 or 334).

Each section of the DC003 contains an internal "interrupt enable" flip-flop. The enable in section B is always set, the result of a logic high being continually clocked in; therefore, any time the RQSTB input is asserted by the microprogram an interrupt is requested. The enable in section A can be loaded by the microprogram; the data input is bit 08 of the DAL bus and the loading clock is the CLK STOP ENA H signal (a strobe pulse selected by the Strobe field of the microword). The section A

interrupt enable can be controlled by bits 08 and 09 of the Load Status Register A display instruction: if bit 09 = 1, bit 08 is loaded into the interrupt enable. Thus, the Load Status Register A instruction can cause display processing to stop (bit 10 = 1) either with or without a subsequent STOP interrupt. If a JOYSTICK MATCH interrupt is to be generated, the microprogram sets the enable by asserting DAL 08 and issuing the strobe pulse.

The STOP interrupt sequence proceeds as follows:

1. The Load Status Register A display instruction with bits 08, 09, and 10 all 1, is fetched, specifying a DP stop with interrupt.

2. The microprogram sets the section A interrupt enable.

3. The microprogram sets bit 00, REQ A, of the FLAGS general register (in the 2901A), to indicate that a STOP interrupt is pending.

4. The microprogram proceeds to the Idle-Stop routine, where the STALL flip-flop is cleared in order to block the DEV REPLY signal from passing onto the LSI-11 Bus. In the Idle state, the microprogram must be able to control the issuing of the BRPLY response.

5. Once STALL is clear, the microprogram sets the RQSTA bit in the QBUS Control Register (since the REQ A bit in FLAGS is set), and then proceeds into the Idle loop to await a DEV REPLY (register access or interrupt response).

6. With RQSTA applied, the DC003 asserts BIRQ L (Bus Interrupt Request) on the LSI-11 Bus.

7. BIRQ L is received by the host CPU, and, when conditions permit, the host CPU responds with BDIN and BIAKI (Interrupt Acknowledge In). Because the DP is requesting the interrupt, the DC003 "blocks" BIAKI and prevents it from passing to the next device, thereby assuring that only one device is performing an interrupt at any one time.

8. After BIAKI is received, the DC003 enables the VECTOR H signal and causes the vector address to be asserted onto the LSI-11 Bus. VECTOR H is also applied to the DC004 Protocol circuit, which issues the DEV REPLY signal.

9. In the Idle loop, the microprogram senses the DEV REPLY and VECTOR signals and branches to a routine to handle the interrupt. The interrupt handling routine gates bit 02 of the FLAGS register (in the 2901A array), which for a STOP interrupt is zero, to the DAL bus to supply bit 02 of the vector address. Then it sets the STALL flip-flop to allow DEV REPLY to pass onto the LSI-11 Bus

as BRPLY L. The microprogram then waits for DEV REPLY to negate.

10. When the host CPU receives BRPLY, it reads the interrupt vector and negates BDIN and BIAKI, which in turn causes VECTOR H to be negated, removing the vector from the LSI-11 Bus.

11. Negation of VECTOR H causes DEV REPLY to be negated, allowing the microprogram to clear STALL, RQSTA, the REQ A bit of the FLAGS register, and then return to the Idle loop. The host CPU processes the interrupt vector and enters a routine to service the DP STOP interrupt.

The CURSOR MATCH interrupt sequence proceeds identically to that for STOP, except that bit 02 of the FLAGS register is set, causing bit 02 of the vector to be asserted during the sequence, causing an address of 324 to be generated.

For the ERROR and JOYSTICK SWITCH interrupts, the sequence is again similar, with the exception that bit 01 of the FLAGS register, REQ B, is set in preparation for the interrupt. REQ B causes the Idle-Stop sequence to set RQSTB in the QBUS Control Register, thereby activating section B of the DC003. During interrupt service, bit 03 of the vector address is therefore asserted, causing a vector of either 330 or 334 to be produced depending on the state of the FLAGS bit 02.

4.3.2 Bit-slice Microprocessor Data Paths

The Microprocessor Data Paths section of the Display Processor handles and/or operates upon all data transferred to or from the LSI-11 Bus Interface and the DBUS Interface sections of the DP, under control of the Control ROM and Sequencer logic.

Figure 4-3 is a block diagram of the Microprocessor Data Path. The Data Path is 16 bits wide. Major components are an array of four 2901A 4-bit slice integrated circuits, with carry lookahead and shift linkage, and a 16-word by 16-bit Scratchpad RAM. The 2901A array is an arithmetic-logic unit (ALU) with 17 words of internal data storage. The Scratchpad RAM is comprised of four 16-word by 4-bit random-access memory (RAM) integrated circuits. These augment the storage of the 2901As, thereby providing a total of 33 16-bit words of storage within the DP.

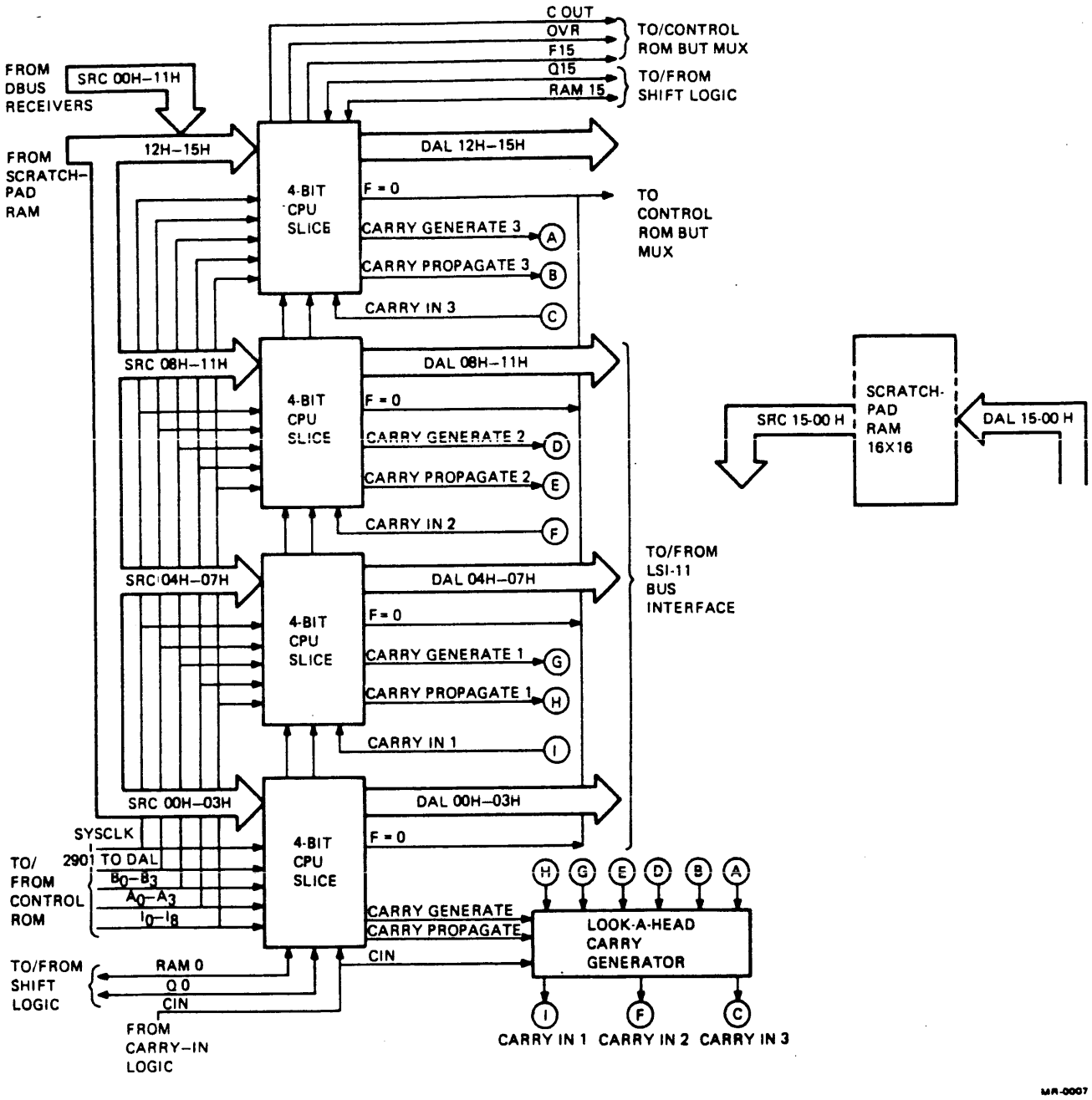


Figure 4-3
16-Bit Slice Microprocessor Block Diagram

4.3.2.1 2901A Bit-Slice Array -

The heart of the 16-bit microprocessor data path is the 2901A 4-bit CPU integrated circuit (IC). The microprocessor can perform addition, subtraction, and five logic functions on two source operands. The 2901A is microprogrammable via three groups of three bits each for source operand selection, arithmetic logic unit (ALU) function, and destination control. These control bits are supplied by the Control ROM via the Pipeline Register (Paragraph 4.3.4). Figure 4-4 is a block diagram of the 2901A microprocessor.

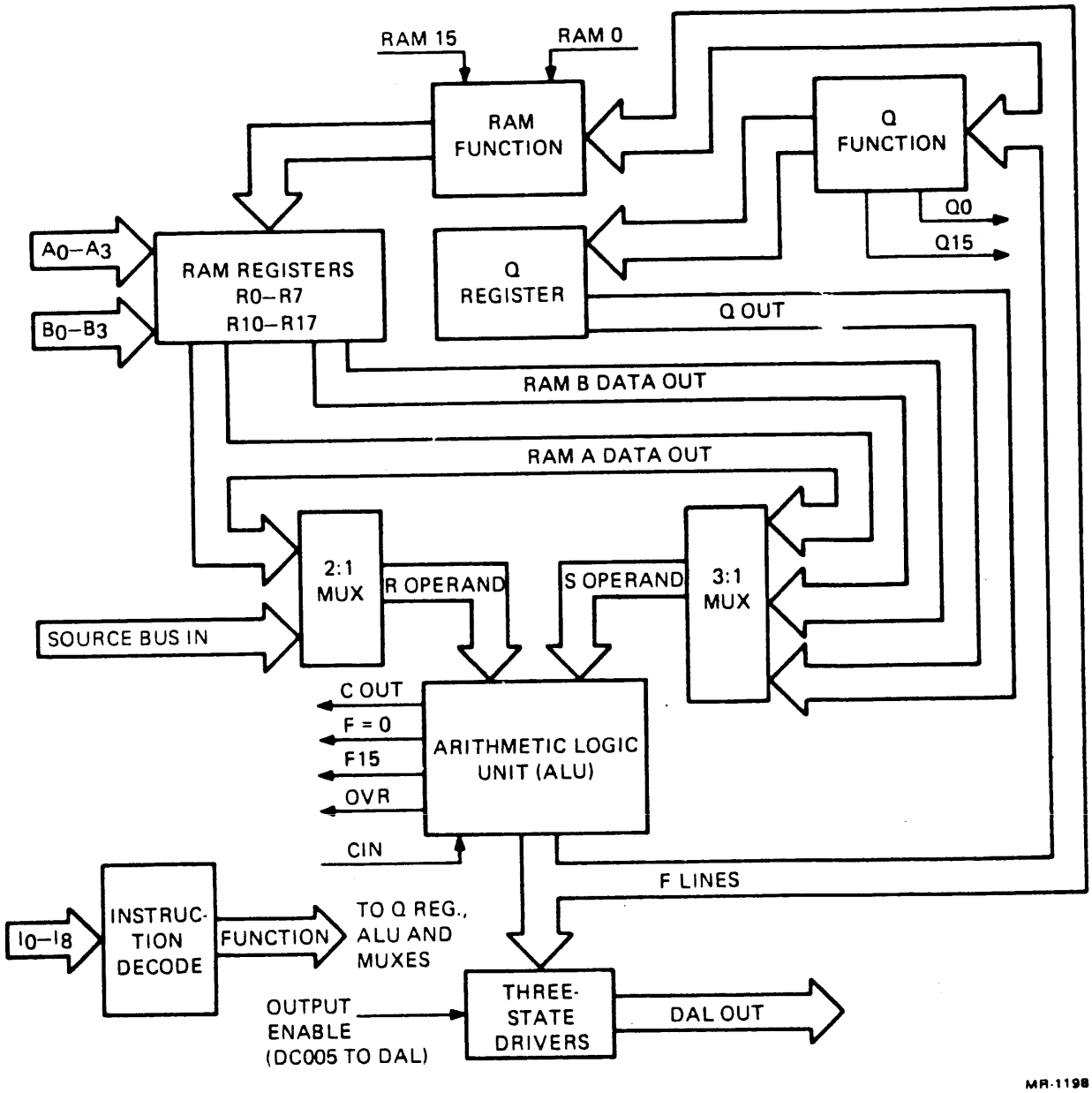


Figure 4-4
2901A Microprocessor Block Diagram

The ALU performs the arithmetic and logic functions. Source operands for the ALU can come from the data input lines (SRC IN), the A RAM register (RAM A DATA OUT), the B RAM register (RAM B DATA OUT), or the Q-REGISTER. The origin of the source operands, as well as the ALU function and ALU resultant destination, is controlled by the I0--I8 instruction lines.

There are 17 registers within the 2901A. The registers include the Q-Register and 16 RAM registers. For the DP, the RAM registers are labeled with their octal codes, R0 through R7, and R10 through R17. A RAM register is selected for reading from or writing to via the four A (A0--A3) or B (B0--B3) lines. The "A" lines can only select RAM registers for reading, but the "B" lines can select registers for both reading and writing; when a write is performed, data is clocked into both the A and B registers.

Each RAM register has an A address (A0--A3 lines) and a B address (B0--B3 lines). These addresses are octal addresses and are the same as the register label; i.e., to address R7 an octal 7 is placed on the A or B address lines. By placing the same address on the A and B address lines, the contents of the addressed RAM register will appear on both the RAM A DATA OUT and RAM B DATA OUT lines. However, only the RAM B address lines can select RAM registers for writing. (The Q-Register can also be written.) The RAM register labels, their assigned Display Processor function, and their octal addresses are shown in Table 4-1. RAM registers R0, R1, R1, and R3 are addressable from the LSI-11 Bus, as DPC, DSR, DXR, and DYR, respectively.

As previously mentioned, the microinstruction placed on the I lines (I0--I8) determines the origin of the source operands to the ALU, the function which the ALU performs, and where the result of that function is stored. The I lines are encoded with an octal microcoded instruction for the functions shown in Table 4-2.

The ALU destination control (I6, I7, I8) specifies where the output of the ALU (F lines in Figure 4-4) will be stored. The destination can either be the Q-Register or a B RAM register. I6 through I8 also specify the type of function that is performed by either the RAM function or the Q-register function. RAM and Q functions can shift up or down or just transfer the output of the ALU for storage in the Q or RAM registers. When the RAM function is an up or a down shift, RAM 0 (IN0) or RAM 15 (IN15) are employed. RAM 0 and RAM 15 correspond to the least significant bit (LSB) and most significant bit (MSB) of the RAM shift function respectively. The octal microcode for the I5 through I8 lines is listed in Table 4-3. In this table, F refers to the F line DAL bus driver output from the ALU (Figure 4-4), B is a particular B RAM register as selected by the B lines, and Q is the Q-Register.

Table 4-1
2901A RAM Register Assignments

RAM Register	Mnemonic Name	A or B Address (Octal)	Function
R0	DPC*	0	Display Program Counter
R1	DSR*	1	Display Status Register (Opcode, Pixel Data, STOP Flag)
R2	XSR*	2	X Status Register (DXR on LSI-11 Bus) (X-Coordinate of graphic position, joystick cursor or joystick match)
R3	YSR*	3	Y Status Register (DYR on LSI-11 Bus) (Y-Coordinate of graphic position, joystick cursor or joystick match)
R4	FLAGS**	4	Pending interrupt flags and Graphic-Mode Op-Code. Also used as temporary storag
R5	PMASK	5	Memory Protection Mask for currently active segment.
R6	RELOC	6	Memory Relocation bits 15-09 for currently active segment.
R7	RXA	7	Memory Relocation bits 17-16 for currently active segment. Also contains the Current Segment flag and other flags.
R10	XPOS	10	X Position (X Coordinate of current graphic position, in 512-point resolution format)
R11	YPOS	11	Y Position (Y Coordinate of current graphic position, in 512-point resolution format)

(continued on next page)

* Register can be accessed from LSI-11 Bus.

** Register can be accessed from LSI-11 Bus via DSR location.

Table 4-1 (cont'd)
2901A RAM Register Assignments

RAM Register	Mnemonic Name	A or B Address (Octal)	Function
R12	TEMP0	12	Temporary Hold No. 0.
R13	TEMP1	13	Temporary Hold No. 1.
R14	TEMP2	14	Temporary Hold No. 2.
R15	COUNT	15	Iteration counter for pixel-writing loops (vector generation and bit-map). Also used for temporary storage.
R16	AC	16	Accumulator for vector slope control. Also used for temporary storage.
R17	TAN	17	Tangent of vector angle. Also used for temporary storage.

Table 4-2
2901A I Line Functions

I Lines	I<8:6>	I<5:3>	I<2:0>
FUNCTION	ALU Destination Control	ALU Function Control	ALU Source Control

The function F/2 divides the value on the F lines by two (by shifting to the right) and loads the result into the RAM, and Q/2 divides the contents of the Q register by two. Conversely, 2F or 2Q doubles the value of F or Q. An important destination function is the "ALU Bypass" operation, octal code 2 in Table 4-3, in which the ALU output can be stored in the B RAM register while the A RAM register is gated directly to the DAL bus. This is used heavily while writing coordinate and pixel data into Image Memory.

Table 4-3
ALU Destination Control

Mnemonic	Microcode 1876	Octal Code	RAM Function Shift	RAM Function Load	Q-REG Function Shift	Q-REG Function Load	Y Out	RAM Shifter Input RAM0	RAM Shifter Input RAM3	Q Shifter Input Q0	Q Shifter Input Q3
QREG	LLL	0	X	None	None	F>Q	F	X	X	X	X
NOP	LLH	1	X	None	X	None	F	X	X	X	X
RAMA	LHL	2	None	F>B	X	None	A	X	X	X	X
RAMF	LHH	3	None	F>B	X	None	F	X	X	X	X
RAMQD	HLL	4	Down	F/2>B	Down	Q/2>Q	F	F0	IN3	Q0	IN3
RAMD	HLH	5	Down	F/2>B	X	None	F	F0	IN3	Q0	X
RAMQU	HHL	6	Up	2F>B	Up	2Q>Q	F	IN0	F3	IN0	Q3
RAMU	HHH	7	Up	2F>B	X	None	F	IN0	F3	X	Q3

L = Low Logic Level
H = High Logic Level
X = Don't Care condition
B = RAM Register addressed by B Lines
UP is toward MSB
DOWN is toward LSB

It was previously mentioned that the 2901A microprocessor can perform three arithmetic functions and five logic functions. These functions are selected by the microcoded instruction on I lines I3 through I5 . The eight functions are shown in Table 4-4 along with their octal codes for the I lines. This table and Table 4-5 use the symbols R and S to designate ALU source operands.

The source operand control I lines (I lines I0 through I2) determine from where the source operands for the ALU will come. Source operands can come from an A or B RAM register, the Q-Register, or the data input lines (SOURCE BUS IN) to the 2901A. The source operands can also be equal to zero for some codes.

Table 4-6 is a matrix which summarizes the functions of I2, I1, I0 (defines columns in Table 4-6) and I5, I4, I3 (defines rows in Table 4-6).

Since the functions of the I lines are defined in Tables 4-3, 4-4, and 4-5, these tables are used to develop a microcode for the 2901A microprocessor.

Table 4-4
ALU Function Control

Mnemonic	Microcode I5	I4	I3	Octal Code	ALU Function
ADD	L	L	L	0	R plus S
SUBR	L	L	H	1	S minus R
SUBS	L	H	L	2	R minus S
OR	L	H	H	3	R or S
AND	H	L	L	4	R and S
NOTRS	H	L	H	5	-R and S
EXOR	H	H	L	6	R exclusive-or S
EXNOR	H	H	H	7	R exclusive-nor S

L = Low Logic Level
H = High Logic Level
R and S = Source Operands (Table 4-5)

Table 4-5
ALU Source Operand Control

Mnemonic	Microcode				ALU Source Operands	
	I2	I1	I0	Octal Code	R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	0	Q
ZB	L	H	H	3	0	B
ZA	H	L	L	4	0	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	0

L = Low Logic Level
H = High Logic Level
A = RAM A Register
B = RAM B Register
Q = Q-Register
0 = Operand equals 0 (zero)
D = Data In lines (from SRC Bus)

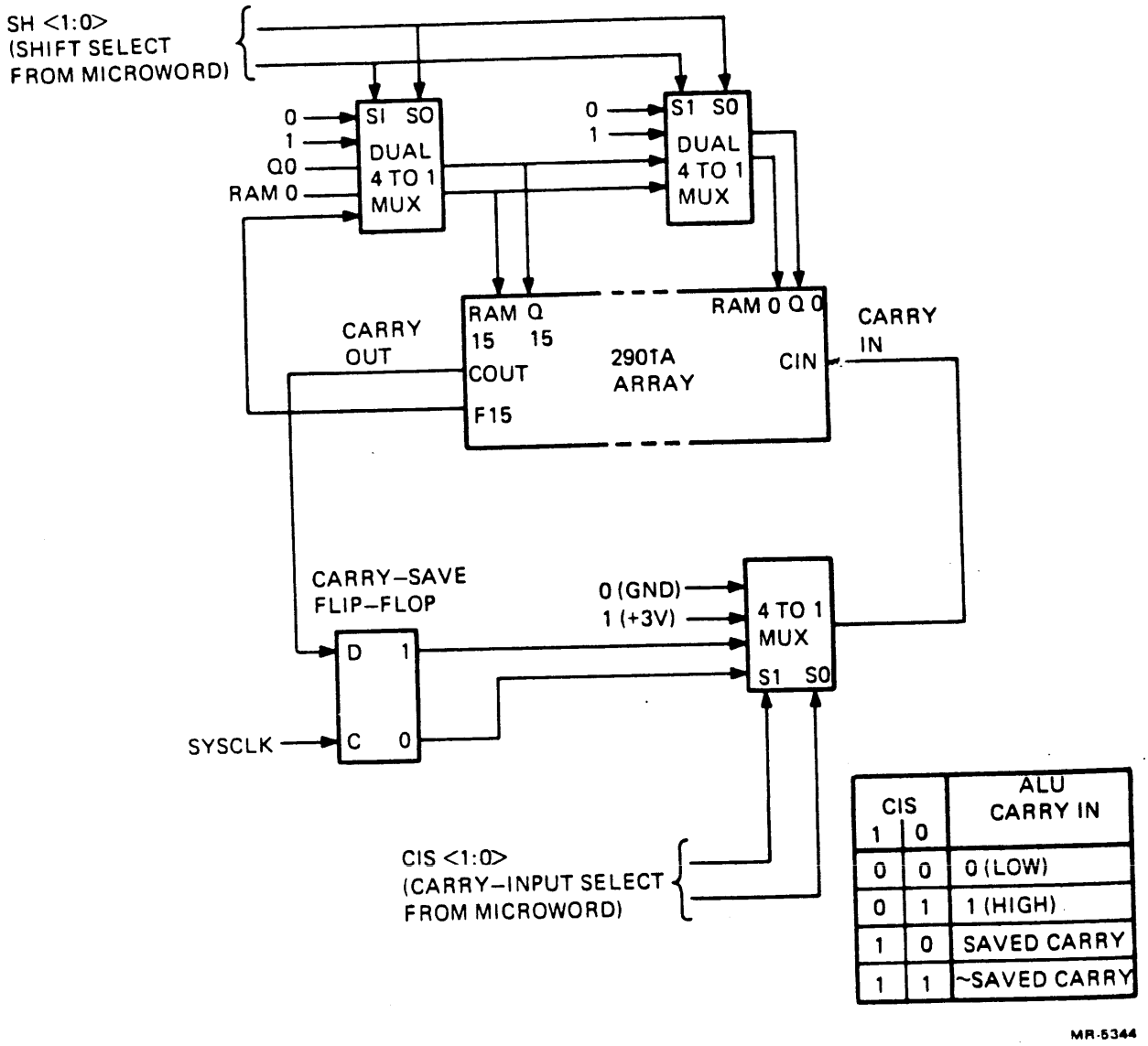
Table 4-6
Source Operand/ALU Matrix

I<2>	I<1>	I<0>	ALU Funct.	ALU Source I<2,1,0> Octal Code 0	1	2	3	4	5	6	7
				A, Q	A, B	0, Q	0, B	0, A	D, A	D, Q	0, D
0	0	0	Ci=L ADD Ci=H	A+Q A+Q+1	A+B A+B+1	Q Q+1	B B+1	A A+1	D+A D+A+1	D+Q D+Q+1	D D+1
0	0	1	Ci=L SUBR Ci=H	Q-A-1 Q-A	B-A-1 B-A	Q-1 Q	B-1 B	A-1 A	A-D-1 A-D	Q-D-1 Q-D	-D-1 -D
0	1	0	Ci=L SUBS Ci=H	A-Q-1 A-Q	A-B-1 A-B	-Q-1 -Q	-B-1 -B	-A-1 -A	D-A-1 D-A	D-Q-1 D-Q	D-1 D
0	1	1	OR	A OR Q	A OR B	Q	B	A	D OR A	D OR Q	D
1	0	0	AND	A AND Q	A AND B	0	0	0	D AND A	D AND Q	0
1	0	1	NOTRS	$\overline{A}$ AND Q	$\overline{A}$ AND B	Q	B	A	$\overline{D}$ AND A	$\overline{D}$ AND Q	0
1	1	0	EXOR	A EXOR Q	A EXOR B	Q	B	A	D EXOR A	D EXOR Q	D
1	1	1	EXNOR	$\overline{\text{A EXOR Q}}$	$\overline{\text{A EXOR B}}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{\text{D EXOR A}}$	$\overline{\text{D EXOR Q}}$	$\overline{D}$

Ci = Carry In to LSB of ALU
L = Low Logic Level
H = High Logic Level
A = RAM A Register
B = RAM B Register
Q = Q-Register
0 = Operand equals 0 (zero)
D = Data In lines (from SRC Bus)
+ = Plus
- = Minus
EXOR = Exclusive-OR

4.3.2.2 Carry-Input And Shift Linkage -

The Carry-Input to the least-significant bit of the 2901A array is supplied by a 4-input multiplexer. Under control of the 2-bit Carry Input Select (CIS) field of the microword, one of four signals can be applied to the 2901A carry input. Figure 4-5 illustrates the carry-input circuit and provides a list of the carry-input microcode functions supplied by the microword (0, 1, and true or inverted Saved Carry from the previous microinstruction).



CIS 1	CIS 0	ALU CARRY IN
0	0	0 (LOW)
0	1	1 (HIGH)
1	0	SAVED CARRY
1	1	~SAVED CARRY

Figure 4-5
Carry-Input and Shift Linkage Logic for 2901A Array

The Carry-Save flip-flop is loaded with the carry out of the most significant bit of the 2901A (bit 15) at the end of each cycle of the microprogram. The "true" or "complement" of this flip-flop can be applied to the carry input via the Carry-Input Multiplexer. This capability facilitates multiple-precision arithmetic operations.

For the addition of two 16-bit numbers, a carry-in of 0 is selected. For subtraction, a carry-in of 1 is used. Increment and decrement operations (in which one of the 2901A ALU source operands is zero) select a carry-in of 1 and 0, respectively. Use of the carry-save inputs allows implementation of "conditional increment" and "conditional decrement" operations. For a conditional increment, the 2901A instruction is configured to add a zero to a selected register, and the true sense of the carry-save flip-flop is selected to supply the carry in. Thus, if a carry out of the 2901A occurred on the previous microinstruction, the selected register will be incremented. For a conditional decrement, zero is subtracted from the selected register, and the complement of carry-save is selected for the carry-in. Thus, the selected register will be decremented if a carry-out occurred on the previous microinstruction.

Shifting of data between 2901A elements occurs over bidirectional lines between the elements under control of the ALU DESTINATION field of the microword (I<8:6>). At the ends of the array, 3-State multiplexers are used to select the data to be entered into the least- or most-significant Q-Register and/or RAM register bits during shift operations. ALU Instruction bit 7, in the ALU DESTINATION field of the microword, selects which multiplexer is active. I7 is low (0) on a shift right; it is high (1) on a shift left. The two-bit SH <1:0> field in the microword selects the particular multiplexer input, as listed in Table 4-7.

Table 4-7
Shift Multiplexer Inputs

SH1	SH0	Function	Description
0	0	ZERO	A logic 0 (low) is applied to the various inputs (Q0, q15, RAM0, RAM15), causing a 0 to be entered into the least- significant (left shift) or most- significant (right shift) register bit.
0	1	ONE	A logic 1 (high) is applied to the register inputs, causing a 1 to be entered into a vacated bit.
1	0	ROTATE	Bits leaving one end of a register are entered into the other end of that same register.
1	1	ARITHMETIC SHIFT	On a right shift, the MSB (sign bit) of the ALU output is entered into the MSB of the RAM; if Q is also shifted (double precision shift) the LSB of the RAM is en ered into Q15. On a left shift, Q15 s entered into RAM 0; if Q is also shifted, 0 enters Q0.

4.3.2.3 Scratchpad RAM -

The Scratchpad RAM is a random-access memory of sixteen words of 16 bits each, constructed of four 16-word by 4-bit chips. Each chip contains four bits of each word. As shown in Figure 4-3, the RAM receives data from the DAL bus and transmits data on the Source (SRC) bus.

The 4-bit Scratchpad Register (SPR) field in the microword selects one of the 16 registers in the RAM to be read and/or written. The contents of the selected register is gated onto the SRC bus if the microword Source-Bus Select field is 0. If the Scratchpad Write bit (SPW) bit is set in the microword, the data on the DAL bus is loaded into the selected register at the end of the current microcycle.

Table 4-8 lists the name and usage of each register in the Scratchpad RAM. Half of the registers are used for short-term storage, such as temporary values or counts used only during the course of processing one display-file instruction. The other

half are used for long-term storage, such as memory-management parameters, Control-Status Register, Histogram and Character base values, etc. that remain static over the course of many display instructions.

Table 4-8
Scratchpad RAM Register Assignments

RAM	Name	Function/Use
0	MBUF	"Memory Buffer." Transmits extended address bits (16 and 17) and WTBT signal to LSI-11 Bus; receives data from the LSI-11 Bus; also used as a temporary holding register.
1	STEMP0	STEMP0 through STEMP4 are used as temporary holding registers during execution of various functions.
2	STEMP1	
3	STEMP2	
4	STEMP3	
5	STEMP4	
6	XSAVE	XSAVE and YSAVE are used to hold the final X and Y positions, respectively, to be attained during execution of Filled Histogram and Bit-Map graphic operations.
7	YSAVE	
10	MAINMM*	Main Segment Memory Management parameters. Bits 15-12 hold the protection mask, while bits 11-00 hold the relocation value, as specified by the operating software via access through the DSR.
11	AUXMM*	Auxiliary Segment Memory Management parameters. Similar to MAINMM but holds the parameters for the Auxiliary display-file segment.
12	CSR*	Control-Status Register. Contains control and error bits, as specified in Paragraph 3.3.2.4.

(continued on next page)

* Register can be accessed from the LSI-11 Bus via the DSR Register (Chapter 3).

Table 4-8 (cont'd)
Scratchpad RAM Register Assignments

RAM	Name	Function/Use
13	GHINCR	Graph/Histogram Increment Register. Bits 04-00 hold the increment value as specified in bits 05--01 of the LOAD GRAPHPLOT INCREMENT display instruction (Paragraph 3.5.2.12). Bit 06 holds the Pixel Data Inhibit control bit, as specified by the LOAD PIXEL DATA INHIBIT instruction. Bits 15--08 are used to save the character from the high byte of a display-file Character Data Word.
14	HBASE*	Histogram Base register. Bits 08-00 hold bits 09-01 of the value specified by the SET HISTOGRAM BASE display instruction. Bits 15 and 14 hold the Main- and Auxiliary-Segment Write-Protect bits, respectively.
15	CBASE*	Character Base register. Holds the value specified by the SET CHARACTER BASE instruction.
16	PCSAVE*	Display Program Counter Save register. Saves the contents of the DPC during subroutines and Bit-Map processing.
17	JGINST	Contains the microprogram address of the start of the current Graphic Mode processing routine. Also saves the current Graphic Mode Op-Code.

* Register can be accessed from the LSI-11 Bus via the DSR Register (Chapter 3).

The Scratchpad RAM provides the path whereby data from the LSI-11 Bus can be transferred into the 2901A array. For example, during a Data-Out into one of the VSV11's addressable device registers, the data being written (presumably by the host CPU) is gated from the LSI-11 Bus DAL lines, onto the internal DAL bus, and is loaded into the MBUF Scratchpad register. In a subsequent microcycle, the contents of MBUF is gated onto the SRC bus and transferred into the 2901A. A similar sequence is performed when the VSV11 fetches display-file words from the host CPU memory.

The MBUF register in the Scratchpad RAM is also used during each DMA cycle to hold the two high-order address bits for the memory location being addressed. During the address portion of the DMA cycle, MBUF is gated onto the SRC bus. Bits 00 and 01 of the SRC bus are then gated to the LSI-11 Bus BAD 16 and BAD 17 (Bus Address 16 and 17) lines while the remaining address bits are supplied by the 2901A via the DAL bus. During a write into host CPU memory, bit 15 of MBUF also supplies the WTBT (Write/Byte) signal to the LSI-11 Bus.

4.3.3 DBUS Interface

Figure 4-6 shows the DBUS Interface section of the Display Processor. The DBUS is a bidirectional bus carrying data, control and status information between the Display Processor module, the Image Memory modules, and the Sync Generator/Cursor Control modules using twenty-six signal lines.

The DBUS is physically implemented as a 40-conductor flat cable connected at the handle end of each module via a 40-pin header.

The twenty-six signal lines used on the DBUS cable are defined as follows:

1. Twelve bidirectional data lines which are driven and received by the Display Processor.

2. Nine control lines driven by the Display Processor and received by the Image Memories and the Sync Generators.

3. Two status lines driven by the Image Memories and received by the Display Processor.

4. Three status lines driven by the Sync Generators and received by the Display Processor.

Table 4-9 describes the function of each signal line.

As shown in Figure 4-6, the DBUS Data lines are supplied with data from bits 00-12 of the internal DAL bus. They are received and gated onto bits 00-12 of the internal SRC bus. Control signals are supplied by the DBUS Control Register (DBC) which is loaded from bits 08-15 of the EMIT field of the microword. Status signals received from the DBUS are applied directly to the Branch-uTest (BUT) Multiplexer in the Sequencer section of the Display Processor. The following paragraphs describe the action of these various elements during communications with Image Memories and Sync Generators.

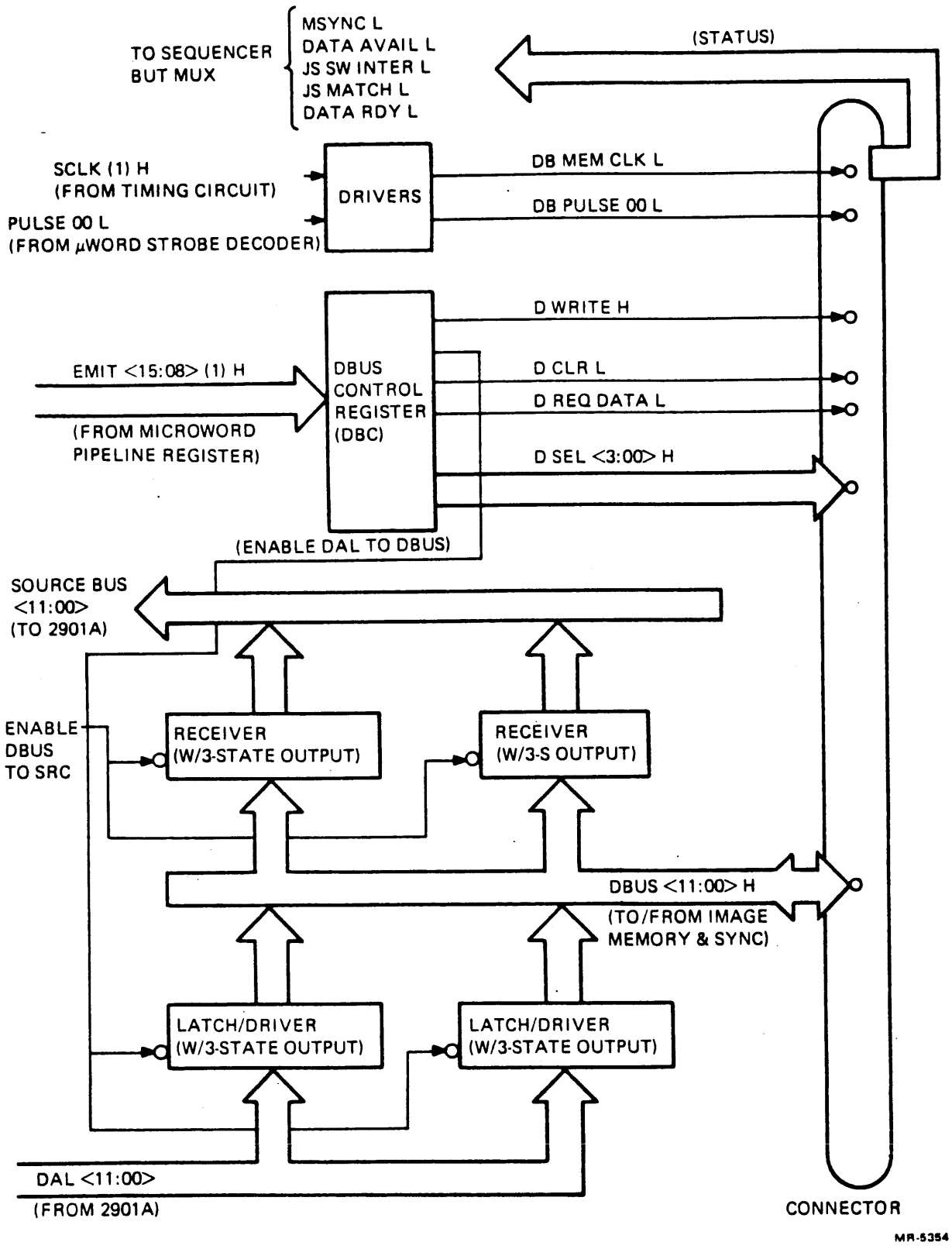


Figure 4-6
DBUS Interface Block Diagram

Table 4-9
DBUS Signal Line Functions

Name	Direction	Description
DBUS <11:00>	Bidirectional	(a) X and Y coordinate data to Image Memories, specifying the coordinates of a pixel location to be written or read back. (b) Pixel Data to be written into Image Memory, specifying the color/intensity of a pixel. (c) Control information to be loaded into the Image Memory control register, specifying the memory operating modes. (d) X and Y coordinate data to be loaded into the Cursor Coordinate registers on a Sync Generator, specifying the position of the cursor crosshairs. (e) Control information to be loaded into the Joystick Control registers on the Sync Generators. (f) Pixel data read from Image Memory during a Pixel Readback operation. (g) Joystick cursor coordinate data and status returned to the Display Processor during a Joystick Status Read operation.
D SEL <03:00>	DP to Image Memory and Sync Generator	This 4-bit Select code specifies a particular register to be accessed or operation to be performed in an Image Memory or Sync Generator.

(continued on next page)

Table 4-9 (cont'd)
DBUS Signal Line Functions

Name	Direction	Description
D PULSE 00	DP to Image Memory and Sync Generator	Strobe pulse, issued with the Select code on D SEL <03:00>, causing the selected register to be written or operation to be initiated.
DB MEM CLK	DP to Image Memory and Sync Generator	Continuous clocking signal causing all Image Memories to be synchronized to the display processor microcycle. Also received by the Sync Generator to synchronize display of the cursor.
D WRITE D CLR D REQ DATA	DP to Image Memory	Cause write-enabled Image Memories to perform a Write cycle, a Clear, or Pixel Readback cycle.
MSYNC	Image Memory to DP	Issued by write-enable Image Memories to indicate that writing of pixels can occur.
DATA AVAILABLE	Image Memory to DP	Issued by Image Memory during Pixel Readback cycle to indicate that the pixel data from the selected location has been placed on the DBUS Data lines and can be read by the Display Processor.
JS SW INTR	Sync Generator to DP	Issued by a Sync Generator when the Joystick Switch is closed and the Joystick Switch interrupt is enabled.
JS MATCH	Sync Generator to DP	Issued by a sync generator when the Match Interrupt is enabled and the DP has written into an Image Memory location whose coordinates match the current position of the joystick cursor.
DATA RDY	Sync Generator to DP	Issued by Sync Generator to indicate presence of X or Y cursor data on DBUS Data lines during a Joystick Status read cycle.

4.3.3.1 DBUS Data Drivers And Receivers -

The DBUS Data drivers consist of two transparent latch chips with 3-state outputs. The output-enable for these chips is controlled by bit 14 of the DBUS Control Register (Paragraph 4.3.3.2). When the output-enable is low, the chips are actively driving data onto the DBUS. When the output-enable is high, the drivers are placed in a high-impedance state and so do not affect the DBUS. When the latch-enable input is high, it allows data on the DAL <11:00> bus inputs to pass to the latch outputs. Bringing the latch-enable low causes the output data to be held stable. This occurs during the last 40 nanoseconds of one microcycle and the first 40 nanoseconds of the next microcycle to allow for tail-end deskewing of DBUS data.

Data to be written into a register of the Image Memory or Sync modules is typically held in one of the registers in the 2901A array. When the data is being written the microprogram performs the following, typically within one microinstruction:

1. The EMIT <11:08> bits are configured with the appropriate D SEL code to select the Image Memory or Sync register being written. EMIT bit 14 is specified as zero to enable the DAL data to be gated onto the DBUS. The ENABLE DBC bit in the microword is coded as a one to allow the DBUS Control Register (DBC) to be loaded with the EMIT data.

2. The microword is coded to select a 2901A register and gate its contents onto the DAL bus.

3. The data passes from the DAL bus onto the DBUS and is presented to the Image Memory and Sync registers.

4. The microword is coded to cause the PULSE 00 strobe to be issued. When the selected memory or sync register receives this pulse, the data is loaded into the register and the cycle is complete.

When data is being read from a Memory or Sync register, the read operation is triggered by a previous microprogram operation, which varies depending upon the source of the data. The microprogram sets bit 14 of the DBC to disable the DBUS data drivers, forcing them into a high-impedance state. The microprogram then waits for a signal from the Memory or Sync indicating that the requested data has been placed on the DBUS Data lines. If the data is coming from an Image Memory, the microprogram waits for the DATA AVAILABLE status signal. If data is being read from a Sync module, the wait is for assertion of DATA READY. When the required signal is received, the microprogram enables the DBUS Receivers to gate the data onto the Source (SRC) Bus. From the SRC Bus, the data is loaded into a register in the 2901A. After data is loaded, the microprogram signals the completion of the cycle to the Image Memory or Sync, which removes its data from the DBUS.

4.3.3.2 DBUS Control Register (DBC) -

The DBUS Control Register (DBC) is an 8-bit register, loaded from bits 08--15 of the EMIT field of the microword when the Enable DBC Load (EN DBC) bit in the microword is set. Figure 4-7 illustrates the DBC bit format, and Table 4-10 describes each bit.

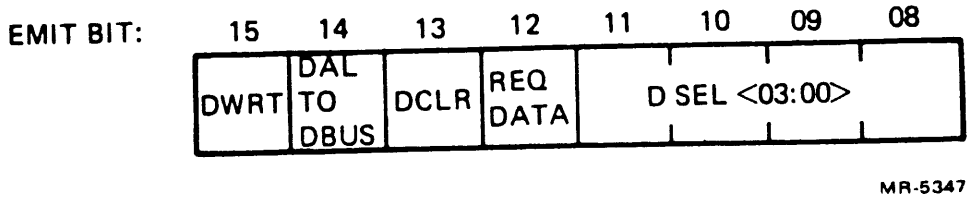


Figure 4-7
DBUS Control Register Format

Table 4-10
DBUS Control Register Bit Definitions

EMIT Bit	Name	Description
15	DWRT (D WRITE H)	When set (1), causes pixel write cycles to be initiated in all write-enabled Image Memories.
14	DAL TO DBUS	When clear (0), the DBUS Data drivers are enabled and DAL Bus data is gated onto the DBUS data lines. When set (1), the drivers are inhibited.
13	D CLR	When clear (0), causes the D CLR L signal to be sent to all Image Memories. This bit is held clear, while the DWRT bit is held set, for a minimum of one full display field time to clear all write-enabled Image Memories.
12	REQ DATA (Request Data)	When clear (0), and the DWRT bit is set, a Pixel Readback cycle is triggered in all write-enable Image Memories. The memory reads the pixel data at the X-Y position previously loaded, places the data on the DBUS Data lines, and asserts DATA AVAILABLE.

(continued on next page)

Table 4-10 (cont'd)
DBUS Control Register Bit Definitions

EMIT Bit	Name	Description
11-08	D SEL <03:00> (DBUS Register Select, bits 03-00)	This 4-bit field is encoded to select an action or register in an Image Memory or Sync module; the specified action is performed when the PULSE 00 is issued by the microprogram. The D SEL codes are:
	Code	Action
	0	Terminate CURSOR READBACK cycle
	1	Write JOYSTICK STATUS Register
	2	Write Image Memory X Position
	3	Write Image Memory Y Position
	4	Write Image Memory Status Register
	5	Write Image Memory Pixel Data Latch
	6	Perform mode switch in enabled Image Memories
	7	Unused
	10	Trigger reading of cursor X and Y coordinates on SYNC channel with Joystick Interrupt pending
	11	Trigger reading of cursor X coordinate on the SYNC channel selected by DBUS Data bits 11-10
	12	Trigger reading of cursor Y coordinate on the Sync channel selected by DBUS Data bits 11-10
	13	Write cursor X coordinate
	14	Write cursor Y coordinate
	15	Write Extended Cursor Control Register (Blink and Switch bits)
	16, 17	Unused

4.3.4 Control ROM, Sequencer And Timing

Operation of the entire Display Processor is under control of a microprogram residing in the Control ROM (Read-Only Memory). Control of the microprogram sequence itself is also provided by the ROM. Figure 4-8 is a block diagram of the ROM, its pipeline (output buffer) register, and the microprogram sequencing logic. The basic elements in this control section are described in Table 4-11.

The following paragraphs provide details of the various elements within the control section.

Table 4-11
Control ROM Basic Elements

Name	Description
ROM	Read-Only Memory. The ROM is an addressable nonvolatile memory containing 1024 words of 64 bits each. The ROM is composed of sixteen 1024 X 4-bit ROM ICs. The ten input address lines to the sixteen ROMs are wired in parallel, thus selecting one 64-bit control word at a time.
PIPELINE REGISTER	The Pipeline Register stores all 64 bits from the ROM. The outputs from this register are then applied to the other elements in the DP to control their operation. The content of the Pipeline Register is termed the current microword or microinstruction, since it is the control word presently acting upon the other elements. The ROM output is termed the next microword. The timing is such that the next microword is always being accessed from the ROM while the current microword is executing, allowing the DP to run at maximum speed.

(continued on next page)

Table 4-11 (cont'd)
Control ROM Basic Elements

Name	Description
2909 SEQUENCER	The set of three 2909 Sequencer ICs provides the ten microprogram address lines to the ROM; each 2909 supplies 4 bits (2 bits are currently unused). The 2909 Sequencer controls and issues microprogram addresses in response to control signals in the current microword (Pipeline Register). Under microword control, the 2909s can cause the microprogram to continue from one instruction to the next, jump, jump to a subroutine (while saving the next address on an internal stack), and return from subroutine (jumping to an address saved on the internal stack).
BUT MUX (Branch Microtest Multiplexer) and CONDITIONAL CONTROL	The BUT MUX allows the microprogram to select one of 32 conditions for testing, for the purpose of modifying the sequencing of microinstructions. The output of the BUT MUX feeds the SEQUENCER CONDITIONAL CONTROL logic, which, when enabled by the microword, either blocks or passes the microcoded sequencer commands to the 2909s. A condition is tested (via BUT MUX selection) in one microinstruction, and in the next microinstruction a conditional sequencer operation (typically a JUMP) is invoked, specifying the "sense" of the condition being tested. Then, if the condition tested was in one state, the JUMP will be executed and microprogram control will be transferred to another location. If the condition was in the other state, no JUMP occurs and the microprogram continues in sequence.
TIMING	The DP receives the Video Bus backplane signal BCLK (Bus Clock) to derive all of its timing. BCLK is a square wave with an 80ns period. A flip-flop, SCLK, divides this by 2 to obtain a signal with a period of 160 ns, the basic cycle time of the DP. SCLK is buffered and the resulting signal, SYSCLK, is distributed to the logic elements within the DP.

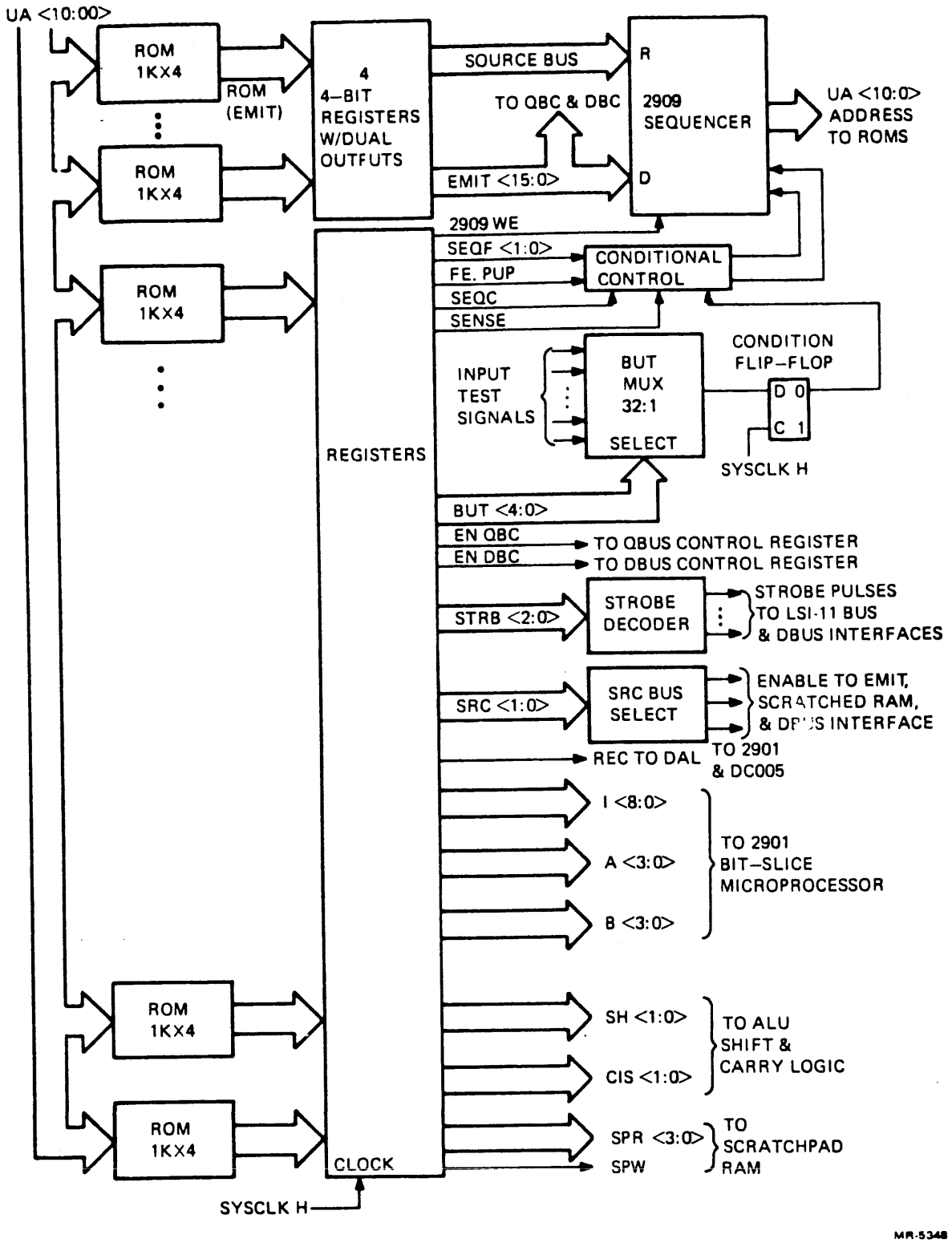


Figure 4-8
Control ROM Block Diagram

4.3.4.1 Basic Machine Cycle Timing -

Timing in the Display Processor (DP) is referenced to the rising edge of the 160 nanosecond SYSCLK signal. The period of SYSCLK therefore defines one microcycle, the time it takes to execute one microinstruction from the Control ROM. SYSCLK itself is derived from the backplane Video Bus B CLK signal via a divide-by-2 flip-flop. Figure 4-9 illustrates the timing sequence.

At the rising edge of SYSCLK, the Pipeline Register is clocked, loading it with data accessed from the ROM in the previous cycle. After the register outputs are settled, they begin acting upon the various elements in the DP. Some of the Pipeline Register outputs control the 2909 sequencer, which provides the address to the ROM for the next microinstruction. At about the halfway point through the cycle (falling edge of SYSCLK), the ROM address is valid and the ROM begins to present its output to the inputs of the Pipeline Register. By the end of the microcycle, all operations specified in the microword in the Pipeline Register are complete except for a final clock signal. The clock signal, which causes data to be stored, such as in the 2901A ALU circuits, is provided by the rising edge of SYSCLK. This simultaneously terminates one microcycle and begins the next by clocking the Pipeline Register.

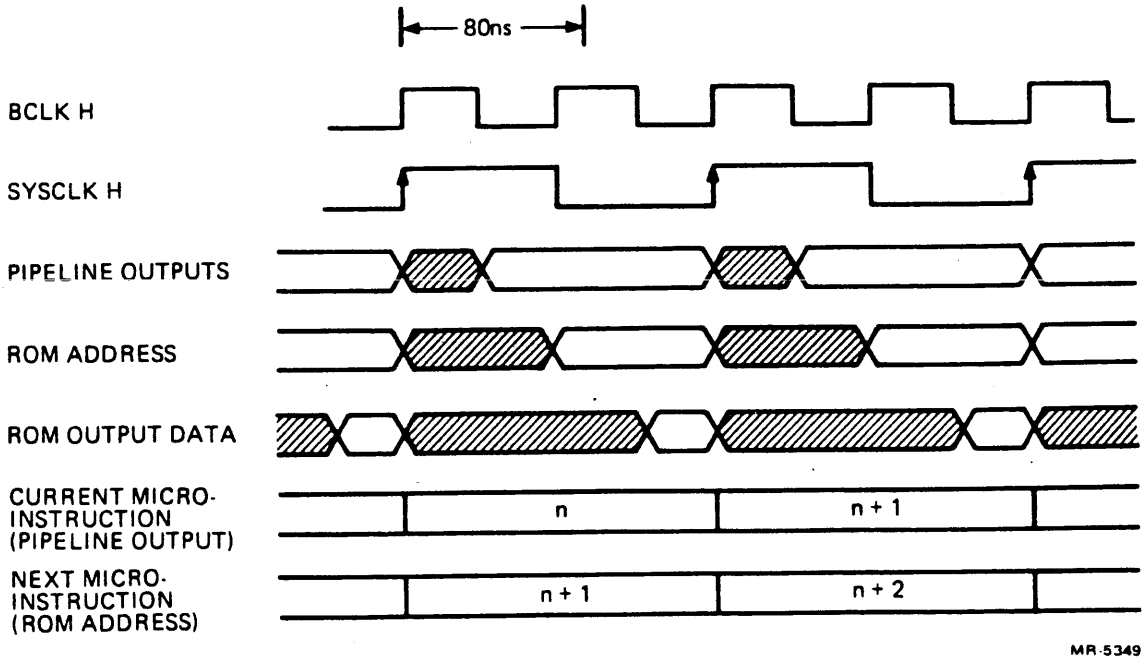


Figure 4-9
Basic Machine Cycle Timing Diagram

4.3.4.2 Microprogram Sequencing -

Words within the control ROM are numbered in sequence, beginning at zero and proceeding up through 1777 (octal). Normally, as in most processors, it is desired to execute ROM words (microinstructions) in numerical order, proceeding from word N to N+1 to N+2, etc. This sequencing is provided for by a "program counter" within the 2909 sequencer circuit. Most of the time, the current microinstruction specifies this sequential mode of operation (via the SEQF -- Sequencer Function -- field). In this mode, the 2909 program counter provides an address to the ROM during the current microcycle. If this address is N, we say that the next microinstruction will be microinstruction N. At the end of the current microcycle, the one executing microinstruction N-1, microinstruction N is available at the ROM outputs and is clocked into the pipeline register to begin its execution. In addition, the 2909 program counter is incremented by 1, to N+1, and begins accessing the ROM.

Occasionally, the microprogram must break the sequential execution of instructions and transfer control to some other ROM location, such as N+100. In these cases, the current microinstruction is coded to cause the 2909 to load a new value, N+100, into its program counter. When this occurs, a "jump" to location N+100 is made, and execution proceeds from there. The new address, N+100, can be supplied from one of three places. In a direct jump, the new address is supplied from the least significant 10 bits of the EMIT field in the current microinstruction. The jump address can also be taken from registers internal to the 2909. In one case, the address can be taken from the internal Address Register, AR. This register is loaded in a previous microinstruction, from the SRC Bus of the display processor, and that SRC data is typically supplied from one of the registers in the Scratchpad RAM. The address data, in turn, was placed in the RAM by the 2901 ALU circuit via the DAL Bus. The third source of jump address information is a pushdown stack within the 2909. Under microprogram control, the contents of the 2909 program counter can be "pushed" onto the stack. This is done for a subroutine call, when it is desired to return to the next instruction following the call.

Figure 4-10 is a simplified block diagram of the 2909 array, which is composed of three 2909 ICs. The 2909 is controlled by five bits in the microword as defined in Table 4-12.

Some combinations of the sequencer function and stack control bits listed above can be given familiar names, as described in Table 4-13.

Table 4-12
2909 Sequencer Microword Control Bits

Bit	Function
ARW	Address Register Write-Enable. When this bit is set, the data on the SRC bus is loaded into the 2909 Address Register at the end of the current microcycle.
SEQF <01:00>*	Sequencer Function. This two-bit field specifies the source of the new ROM address by selecting one of the four multiplexer inputs, as follows:

SEQF <01:00>	Function Name	Address Source	Action
00	CONTINUE	PC	Continue in sequence.
01	JMPR	AR	Jump to the location specified in the Address Register.
10	JMPS	STACK	Jump to the location specified in the top location on the stack.
11	JMPE	D (EMIT)	Jump to the location specified in EMIT.

FE*	File Enable. When this bit is set, the stack is either pushed or popped, as specified by the PUP bit.
PUP*	Push/Pop. When this bit is 0 (and FE = 1), the stack is "popped"; the top word is discarded and the next word rises to the top. When PUP = 1 (and FE = 1), the contents of the PC (microprogram counter) is pushed onto the stack.

* These bits pass through a set of gates to allow their functions to be "conditionalized" (negated if selected conditions are not met).

A processor is worthless if it cannot sense a condition at hand and modify its program flow to take account of the state of that condition. Therefore, the microword provides control bits to facilitate "conditional" sequencer operations. Seven bits in the microword are used for this purpose, allowing a condition to be selected and then conditionaly jumping, calling a subroutine, or returning from a subroutine. If the selected test condition does

not meet the selected criteria, the microprogram merely continues in sequence. The microword bits that control the conditional sequencer operations are described in Table 4-14. The BUT MUX input signals and selection codes are presented in Table 4-15.

Some of the signals tested via the BUT MUX are asserted HIGH i.e., the signal is asserted when it is in the logic HIGH state and negated when it is LOW). Other signals are asserted LOW (negated state is HIGH). Using the SNS (Sense) bit, conditional sequencer action can be taken on either polarity of either type of signal, as described in Table 4-16.

Table 4-13
Sequencer Control Bit Functions

SEQF<1:0>	FE	PUP	Sequencer Instruction
00	0	–	CONTINUE (default condition)
00	1	0	POP: Discard the address on the top of the stack and continue in sequence
00	1	1	PUSH: Push the current PC onto the stack and continue in sequence
01	0	–	JUMPR: Jump via AR (Address Register)
01	1	1	JSRR: Jump to Subroutine via AR
10	0	–	JMPS: Jump via Stack
10	1	0	RTS: Return from Subroutine (JMPS+POP)
11	0	–	JMP or JMPE: Jump Direct via EMIT
11	1	1	JSR or JSRR: Jump to Subroutine via EMIT

Table 4-14
Conditional Sequencing Microword Bits

Bit Name	Function
BUT<04:00>	Branch-Micro-Test. This 5-bit field selects one of 32 conditions to be tested, ranging from constants 0 (logic low) and 1 (logic high), through the status signals provided by 2901A ALU circuits (Carry Out, F = 0, etc.). Included are status signals from the LSI-11 Bus Interface, the DBUS Interface, the VBUS (Video Bus), and several of the DAL Bus data lines. The state of the selected condition is stored in a "condition" flip-flop, where it is acted upon in the next microcycle. Table 4-15 presents the signals and selection codes.
SEQC	Enable Sequencer Conditional. When this bit is set, conditional sequencer operation is invoked. That is, the SEQF <01:00>, FE and PUP control bits are either blocked or allowed to pass to the 2909 sequencer depending on the state of the test condition selected in the previous microinstruction. If the SEQC bit is 0 (unconditional Sequencer function), the sequencer control bits have their stated effect regardless of the state of any condition.
SNS	Test "Sense". This bit selects the sense, or polarity, of the testing operation, selecting the true or complement state of the condition flip-flop for determining whether a condition is met or not met (true or false). When SNS = 0, (and SEQC = 1), the test is met (true) and sequencer action allowed if the tested condition was a logic HIGH; if it was LOW, sequencer action is blocked (program continues in sequence). When SNS = 1 (and SEQC = 1) the test is met and sequencer action is allowed if the tested condition was LOW.

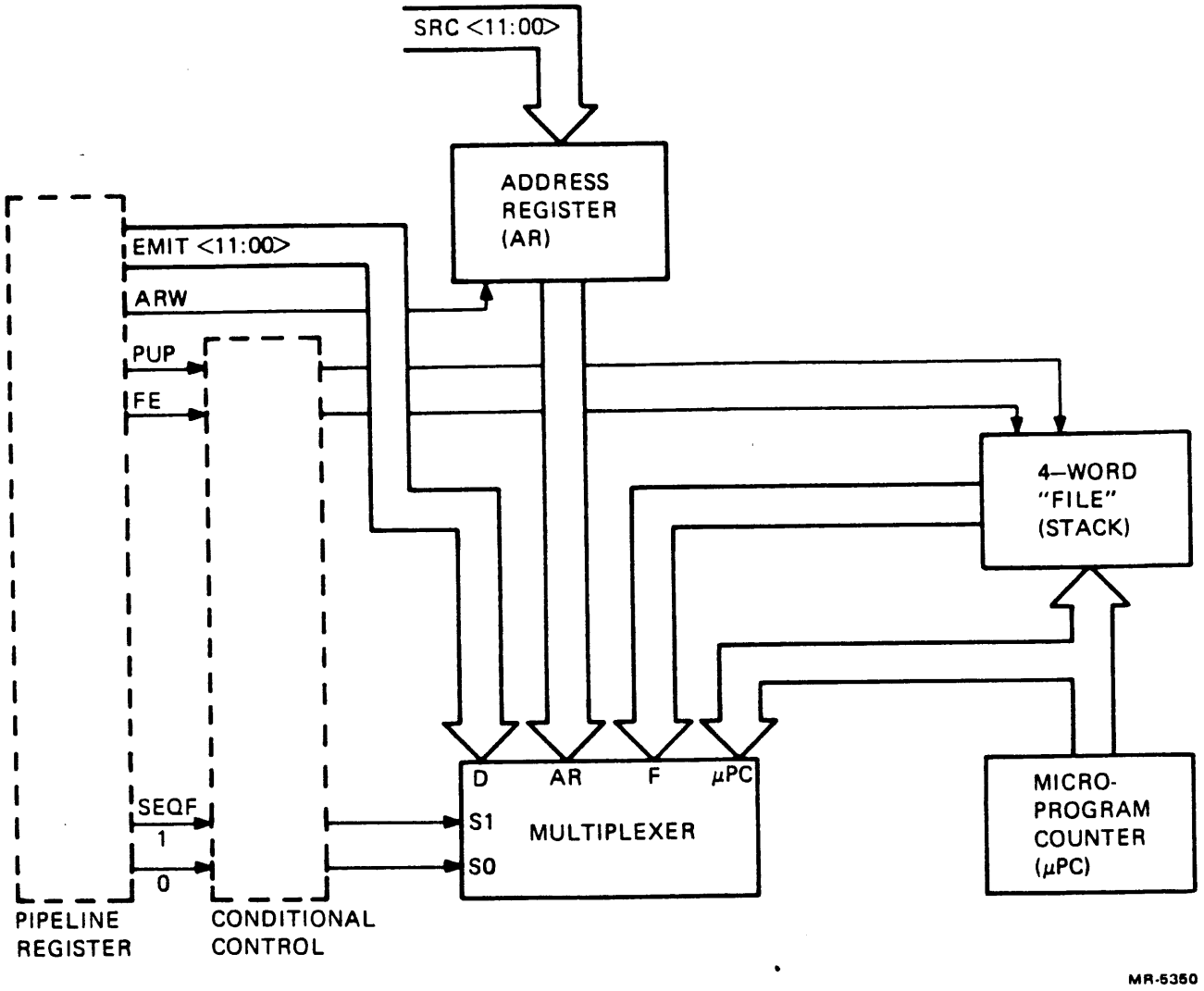


Figure 4-10
2909 Sequencer Simplified Block Diagram

A shorthand notation can be developed to better follow the sequencer operation. If XXX is used to represent a general sequencer operation, such as JMP, JSR, or RTS, then the following notation can be used to describe conditional operation:

Notation	Operation
XXX + HCT	Perform sequencer action if an asserted-High Condition was tested and it was TRUE (High).
XXX + LCT	Perform sequencer action if an asserted-LOW Condition was tested and it was TRUE (Low).
XXX + HCF	Perform sequencer action if an asserted-HIGH Condition was tested and it was FALSE (Low).
XXX + LCF	Perform sequencer action if an asserted-LOW Condition was tested and it was FALSE (High).

Table 4-15
BUT MUX Signals and Selection Codes

BUT<4:0> Octal Code	Signal Name	Description
0	GND	Logic 0 level (Low)
1	+3VB	Logic 1 level (High)
2	VB HBLANK L	Video Bus Horizontal Blank signal. Asserted once per video scan line during horizontal retrace.
3	VB VBLANK L	Video Bus Vertical Blank signal. Asserted once per video field during vertical retrace. Used to time memory Clear and DNOP operations.
4	VB ODD FRM L	Video Bus ODD FRAME signal. Asserted in Interlaced mode during the odd numbered field.
5	VB STALL L	Video Bus STALL signal. For future expansion.
6	RRPLY H	Received BREPLY signal from the LSI-11 Bus.
7	STALL (1) H	Output of the STALL flip-flop in the LSI-11 Bus Interface section of the DP. When clear, blocks DEV REPLY from passing to the bus.
10	MSYNC L	DBUS Sync signal from Image Memory; indicates that pixel writing can occur.
11	JS SW INTR L	DBUS Joystick Switch Interrupt signal; indicates that the switch on the selected Joystick channel has been pressed.
12	JS MATCH L	DBUS Joystick Match signal; indicates that the current pixel writing position matched the cursor coordinates.
13	DATA RDY L	DBUS Data Ready signal from M7061 module; indicates that cursor data is available on the the DBUS.

(continued on next page)

Table 4-15 (cont'd)
BUT MUX Selection Codes

BUT<4:0> Octal Code	Signal Name	Description
14	DATA AVAIL L	DBUS Data Available signal from Image Memory; indicates that pixel data is available on the DBUS Data line during Pixel Readback.
15	BSP1 H	Spare DBUS status signal.
16	EXT STOP (1) H	Flip-flop in LSI-11 Bus Interface section; when set, indicates that the CPU wrote into a VSV11/VS11 register; tested by the microprogram to determine if display processing should be suspended.
17	VB NON-INT L	Video Bus signal indicating that the Image Memories are operating in Non-Interlaced mode.
20 21 22	SEL 0 L SEL 2 L SEL 4 L	Signals from the LSI-11 Bus Interface section indicating the decoded state of the DAL 02 and 01 lines; indicate which device register is being accessed.
23	INWD L	Signal from the DC004 Protocol circuit indicating that a DATI bus cycle is being requested (to read a VSV11 register).
24	DEV REPLY H	Signal from the DC004 Protocol circuit indicating that the VSV11 is being addressed for data transfer.
25	MASTER H	Signal from the DC010 DMA Control circuit indicating that bus mastership has been attained.
26	ENA ST	Signal from the DC003 Interrupt circuit indicating the state of its internal interrupt enable.
27	VECTOR H	Signal from the DC003 Interrupt circuit indicating that an interrupt cycle is in progress (i.e., that the vector is being sent onto the LSI-11 Bus DAL lines).

(continued on next page)

Table 4-15 (cont'd)
BUT MUX Selection Codes

BUT<4:0> Octal Code	Signal Name	Description
30	COUT H	Carry Out signal from the MSB of the 2901A ALU array.
31	OVR H	Arithmetic Overflow signal from the MSB of the 2901A ALU array.
32	F15 H	Sign bit (MSB) of the 2901A ALU array.
33	F=0 H	Signal from the the 2901A ALU array indicating that the number at the output of the ALU is equal to zero.
34	DAL 00 H	Bits from the internal DAL bus.
35	DAL 07 H	
36	DAL 06 H	
37	DAL 09 H	

Table 4-16
Conditional Sequencer Action

Signal Polarity (Asserted)	State As Tested	SNS	Sequencer Action
H	H (True)	0	The specified operation is performed (i.e., JMP, JSR, RTS, etc.).
L	H (False)	0	
H	L (False)	1	
L	L (True)	1	
H	H (True)	1	The specified operation is not performed; the microprogram continues in sequence.
L	H (False)	1	
H	L (False)	0	
L	L (True)	0	

Figure 4-11 is a microprogram flow diagram showing the various sequencer operations. In the diagram, each block represents one microinstruction, executed within one microcycle. Each block, in turn, is divided into three sections. The top section specifies the Sequencer and Conditional functions, the middle section specifies ALU and data-path operations and the third section specifies a condition to be tested via the BUT MUX.

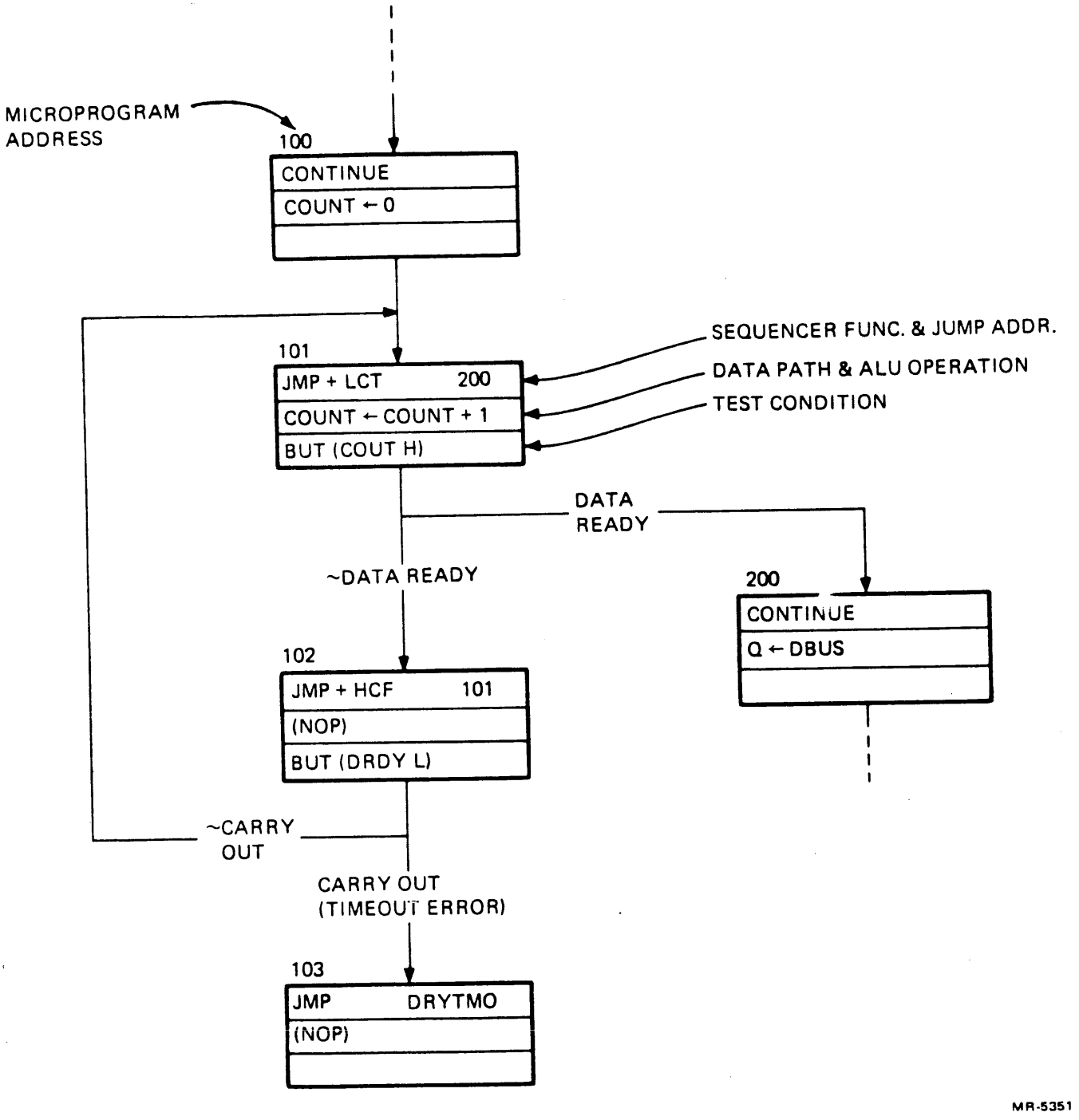


Figure 4-11
Microprogram Flow Example

The program sequence shown is similar to that used for reading data from a cursor position register in a JOYSTICK channel. First, a register in the 2901 (COUNT) is initialized to serve as a "timeout" counter. Then a two-instruction loop is entered to test the DATA READY L (DRDY L) signal while counting (incrementing) the counter. If the Low-true DRDY L condition is seen, the loop is exited with a Jump to read the data from the DBUS into the 2901 Q-Register. If DRDY L is not seen true before 64K cycles through the loop have been made, COUNT is incremented to zero, a CARRY OUT of the 2901 occurs, and the program "falls out" of the bottom of the loop. A Jump is then made to a routine called Data Ready Timeout (DRYTMO) to handle the error.

4.3.4.3 Microword Format -

Figure 4-12 illustrates the format of the 64-bit microword in the Control ROM. Shown also are the IC locations on the M7064 module where each of the 16 ROM circuits resides. Each bit or field has been described previously in terms of the specific logic area it controls. The figure provides a ready reference for the overall microinstruction.

For convenience, the 64-bit microword has been divided into four smaller 16-bit words. Bits have been grouped into the 16-words according to their function, as follows:

WORD 0: ALU Control and QBUS and DBUS Control Register Load-Enable

WORD 1: Register and Bus Selection

WORD 2: Microprogram Sequence Control and Strobe-Pulse Selection

WORD 3: Multipurpose EMIT Field:

(a) 16-bit Constants

(b) Microprogram Branch Address

(c) QBUS Control Data

(d) DBUS Control Data

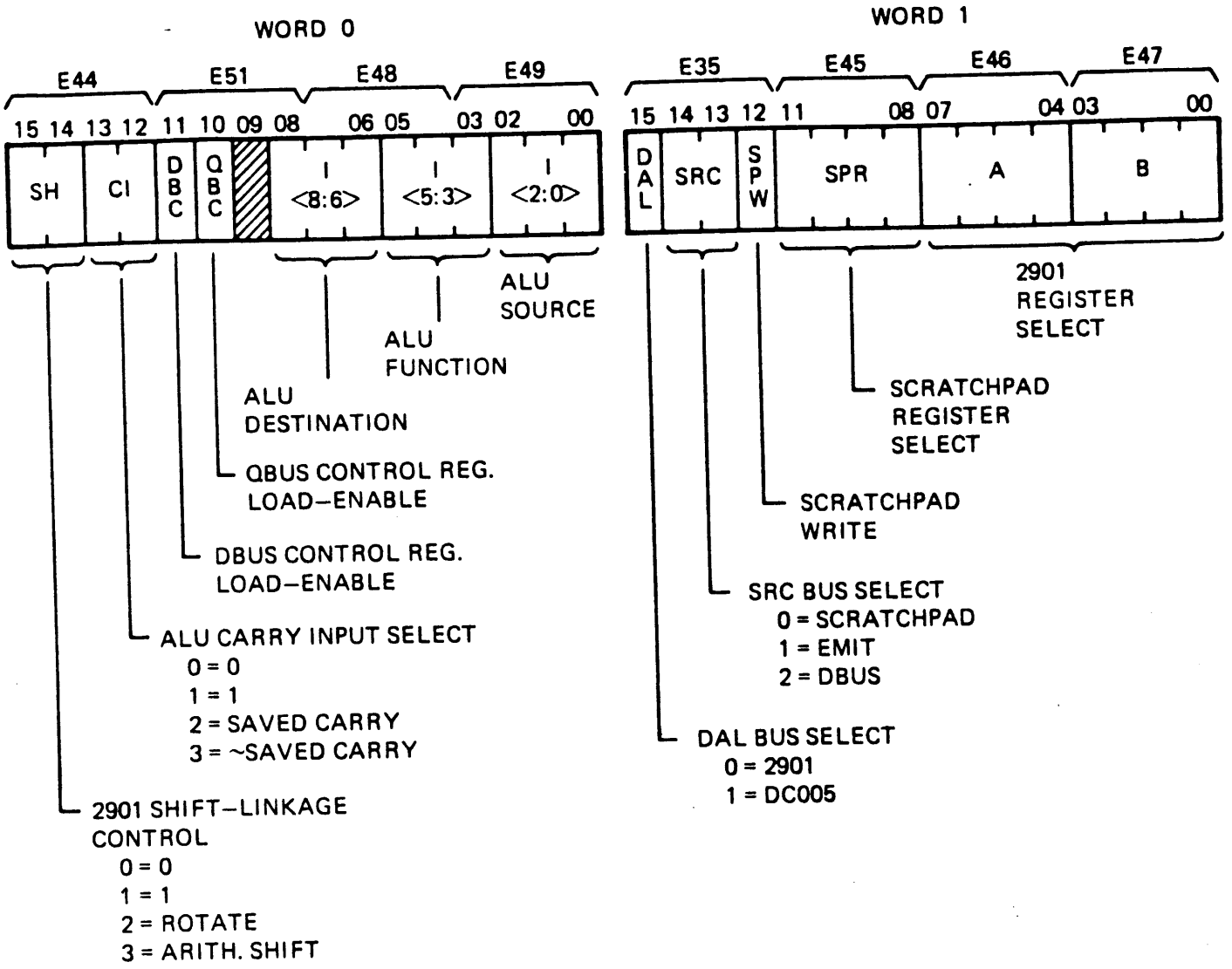


Figure 4-12
M7064 Display Processor Microword Format
(Sheet 1 of 2)

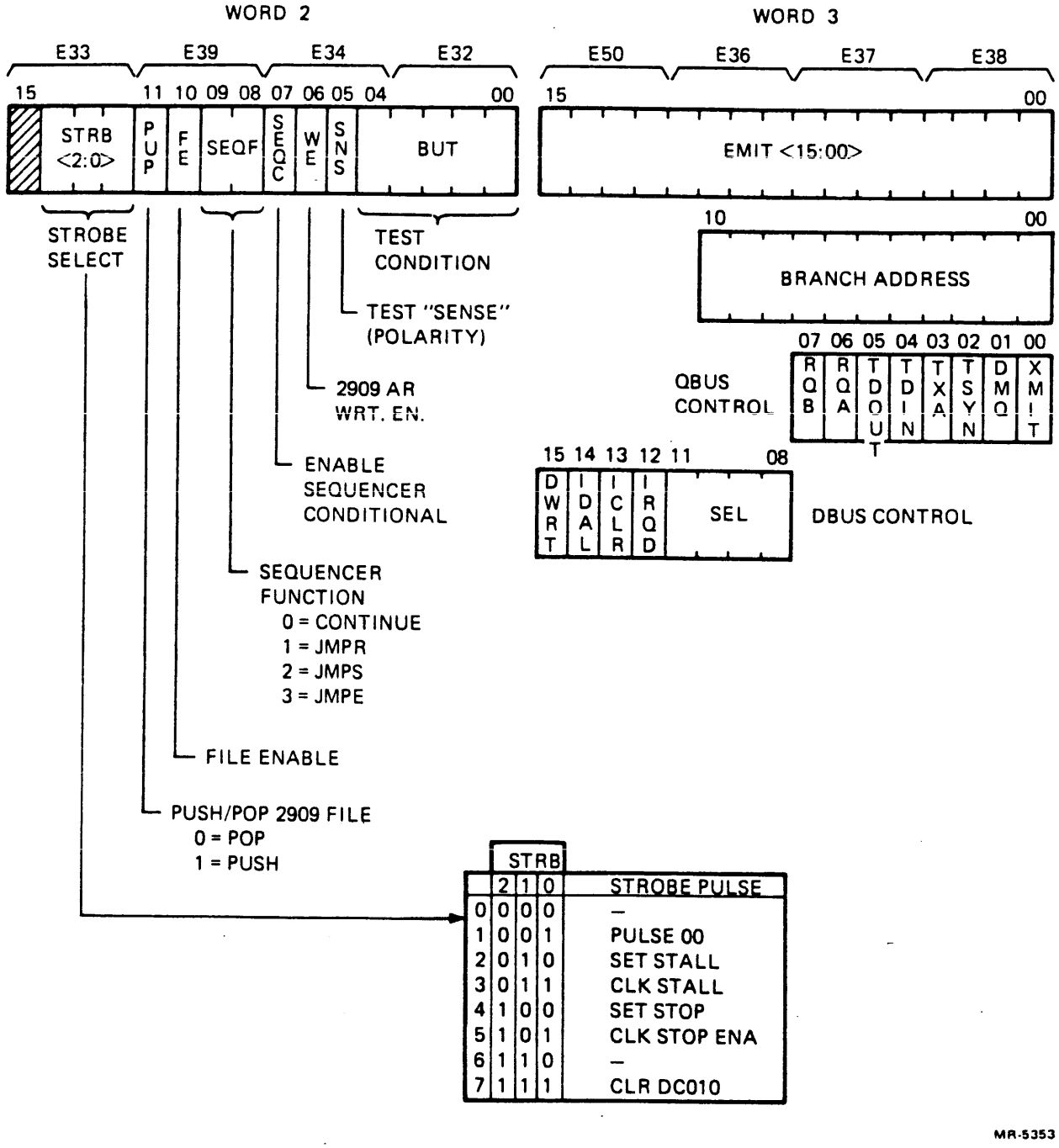


Figure 4-12
M7064 Display Processor Microword Format
(Sheet 2 of 2)

4.4 MICROPROGRAM OVERVIEW

Figure 4-13 is a simplified flow diagram of the Display Processor microprogram. The following paragraphs describe the general operation.

4.4.1 Initialization And Self-Test

The first block of the diagram indicates the Display Processor's Initialization and Self-Test action. This block is entered upon the occurence of the LSI-11 Bus INIT signal or upon writing 100000 (octal) into the DYR register. In this block, various 2901A and Scratchpad registers are cleared or initialzed to a preset value. Then, tests are performed to check the basic integrity of the system: DBUS and VBUS status lines are checked for a "hung" condition (indicating a short or open circuit) and the DBUS Data lines are all tested with a count pattern. If any error is detected, the initialization sequence is aborted and a jump to the appropriate Error Stop routine is made to set an error code into the CSR register.

Assuming all tests are passed, the microprogram proceeds to clear the registers in all available Sync Generator/Cursor Control channels (to disable interupts and turn off the cursor) and sets all Image Memory channels to Write-Only mode. Then, a utility subroutine is called to clear all Image Memories to zero (black). Finally, the program exits to the Idle-Stop block.

4.4.2 Idle-Stop Sequence

In the Idle-Stop section of the program, the microprocessor synchronizes itself to the LSI-11 Bus in preparation to handle accesses to its device registers. Upon entry to Idle-Stop, the microprogram is in the Busy state, with the STALL flip-flop set to allow automatic REPLY to register accesses. In order to service register accesses, the STALL flip-flop must be clear, to block replies until the requested action has been serviced. In addition, a pending interrupt request must be posted (asserted on the LSI-11 Bus) at this time.

First, the FLAGS register in the 2901A is examined. If either the REQ A or REQ B bits are set, the appropriate bit in the QBUS Control Register is set to request the interrupt. Then, the STALL flip-flop is clocked (with the CLK STALL strobe pulse); the data input to the flip-flop is the DEV REPLY signal. STALL is then tested. If it is set, the CPU was trying to access a device register; therefore STALL must be clocked again. The microprogram loops, clocking and testing STALL, until it clears. It then proceeds to the Idle Loop to await action from the LSI-11 Bus, assured that the program is prepared to service any actions.

4.4.3 Idle Loop

In the Idle Loop, the microprogram continually tests the DEV REPLY signal. While it is waiting, it allows LSI-11 Bus BDAL data to be gated onto the internal DAL bus; this allows the DC004 Protocol circuit to decode address bits 1 and 2 for register selection.

DEV REPLY can be asserted either by a register access or by gaining control of the LSI-11 Bus for an interrupt cycle. When DEV REPLY is seen, the VECTOR H signal is tested. If it is asserted, an interrupt service routine is entered to allow gating of the interrupt vector onto the LSI-11 Bus. After the interrupt cycle is complete, the appropriate bits in the QBUS Control Register and FLAGS register are cleared and the program returns to the Idle Loop via Idle Stop.

If the VECTOR H signal was not asserted, the DEV REPLY is for a register access. The microprogram first determines whether the access is for a DATI (Data In, CPU trying to read a VSV11/VS11 register) or for a DATO (Data Out, CPU trying to write into a VSV11/VS11 register). A microprogram branch is taken accordingly.

4.4.4 Data Out Sequence

In the Data Out routine, the microprogram takes the data from the LSI-11 Bus and loads it into the Scratchpad register MBUF. It then copies MBUF into the 2901A Q-Register. It then tests the SEL 0, SEL 2 and SEL 4 signals from the Protocol logic to determine which register is being accessed. A microprogram branch is taken to one of four routines, corresponding to the four device registers.

If the access was for a write into the DPC (SEL 0 asserted), the WRTDPC routine is entered. First, the STALL flip-flop is set to cause BREPLY to be sent onto the bus. Then, bit 0 of the Q-Register is tested to determine if a Start or a Resume is to be performed. If Start, the data in the Q-Register is copied into DPC. Various housekeeping actions are performed (load current Memory Management registers, etc.). Finally, a jump to the Redispatch routine is made to begin display file processing. Upon exit, the STALL flip-flop is allowed to remain set. The microprogram is now in the Busy state.

If the access was for a write into the DSR register, the data in the Q-Register is tested and the appropriate fields written into the selected internal register. After the data is written, STALL is set (to cause BREPLY) and an exit back to the Idle Loop is made. The WRTDSR routine does not cause the DP to go Busy. It also handles its own bus synchronization.

If the DXR or DYR is being written, the DP goes Busy after setting STALL and proceeds to decode the upper bits of the written data to determine what action is to be taken. After the appropriate function has been performed, return to the Idle Loop is made via Idle Stop.

4.4.5 Data In Sequence

If a DATI is being requested, the program gates the data from the selected register onto the internal DAL bus, sets the TXMIT bit in the QBUS Control Register (to cause the data to be driven onto the LSI-11 Bus BDAL lines) and then sets STALL to cause BREPLY. It then waits for DEV REPLY to negate, indicating that the CPU has taken the data. Finally, it clears STALL and returns to the Idle Loop.

4.4.6 Display Processing

Display-file processing begins when the DPC register is written. The entry point is a routine called Redispatch. Redispatch uses the microprogram address stored in the JQINST Scratchpad register to jump directly to the routine responsible for processing the display file. There is one such routine for each Graphic Mode instruction.

Upon initialization, the JQINST register is loaded with the address of the Character Mode routine. However, as processing progresses, other graphic mode instructions are fetched and cause JQINST to be updated to point to the new instruction processing routine.

From Redispatch, the appropriate Graphic Mode routine is entered. The Graphic Mode routine first calls the FNEXT subroutine to fetch the next word from the display file, using the contents of DPC as the virtual address. Before a fetch is begun, however, the FNEXT routine tests for an External Stop condition or a Joystick Switch interrupt. If either of these are present, display processing halts and the program returns to the Idle Loop via a Stop sequence, where interrupts are posted.

Assuming that no stopping condition was detected, FNEXT retrieves a word from memory by calling the FETCH utility subroutine. The word is then tested. If bit 15 is zero (0), the word is a Graphic Mode data word, so a return to the caller is made. If bit 15 of the memory word is one (1), the word is interpreted as an instruction.

When an instruction word is fetched, the Op-Code is decoded to determine if it is a Graphic Mode instruction or a Control or Special instruction. If it is a Graphic Mode instruction, the JQINST register is updated and then used as a dispatch address to

the new Graphic Mode routine. If the instruction is a Control or Special instruction, JGINST is not modified, but a dispatch address is formed (by manipulating the Op-Code bits) and the appropriate processing routine is entered. After the Control or Special instruction is executed, control returns to the current Graphic Mode routine via Redispatch. An exception to this is if the Control instruction was a STATUS A which specified a Stop, in which case the processor returns to the Idle Loop via the Stop sequence.

4.4.7 Utility Subroutines

The microprogram contains a large number of subroutines called from typically many places in the main body of microcode. There are routines to rotate bits within registers, write data into the registers in the Image Memories and Sync Generator/Cursor Control modules, perform DMA cycles to fetch or store data into host CPU memory, manipulate the Memory Management registers, write pixels into Image Memory, draw vectors, and perform various housekeeping tasks.

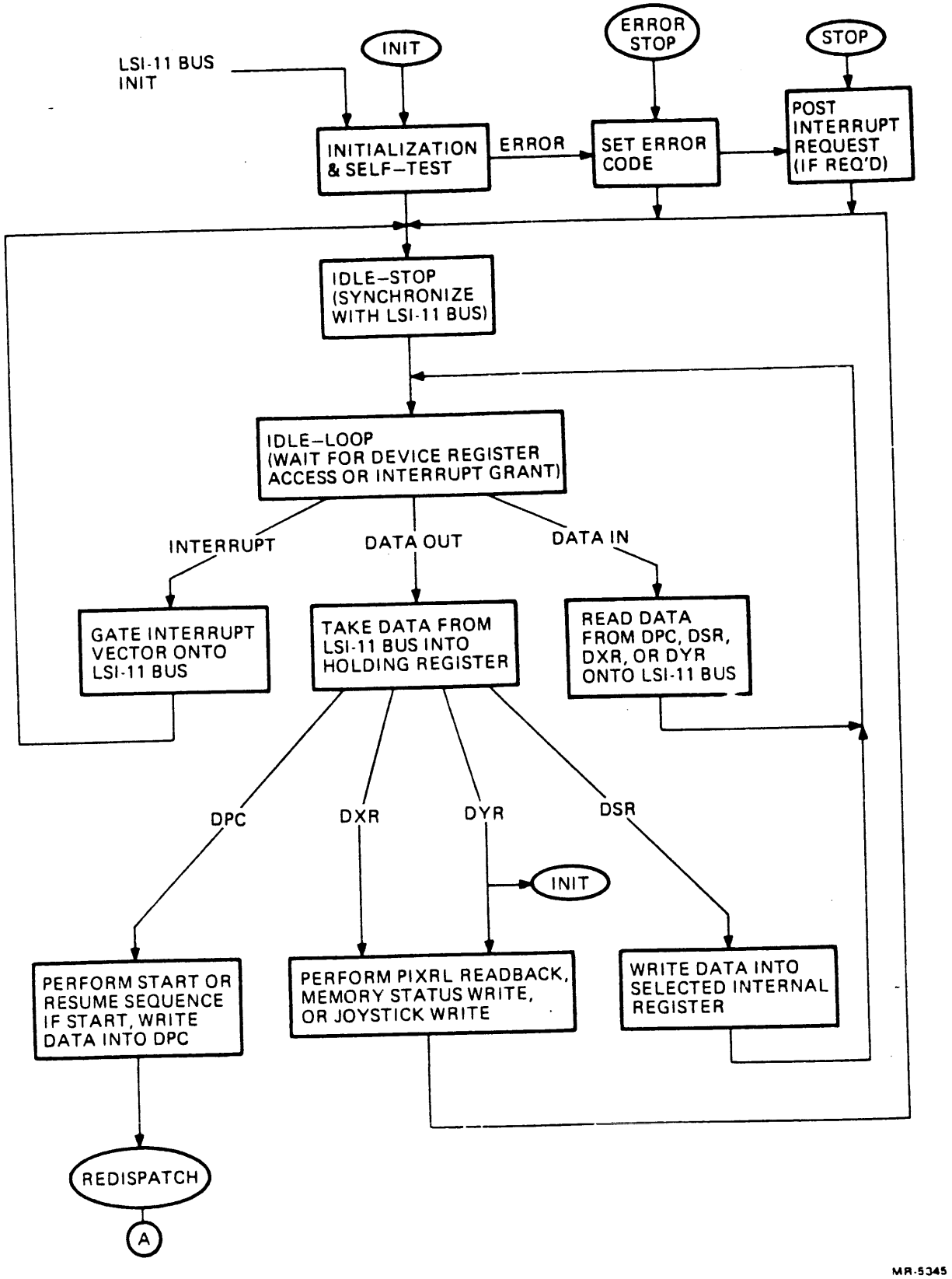


Figure 4-13
Microprogram Overview (Sheet 1 of 2)

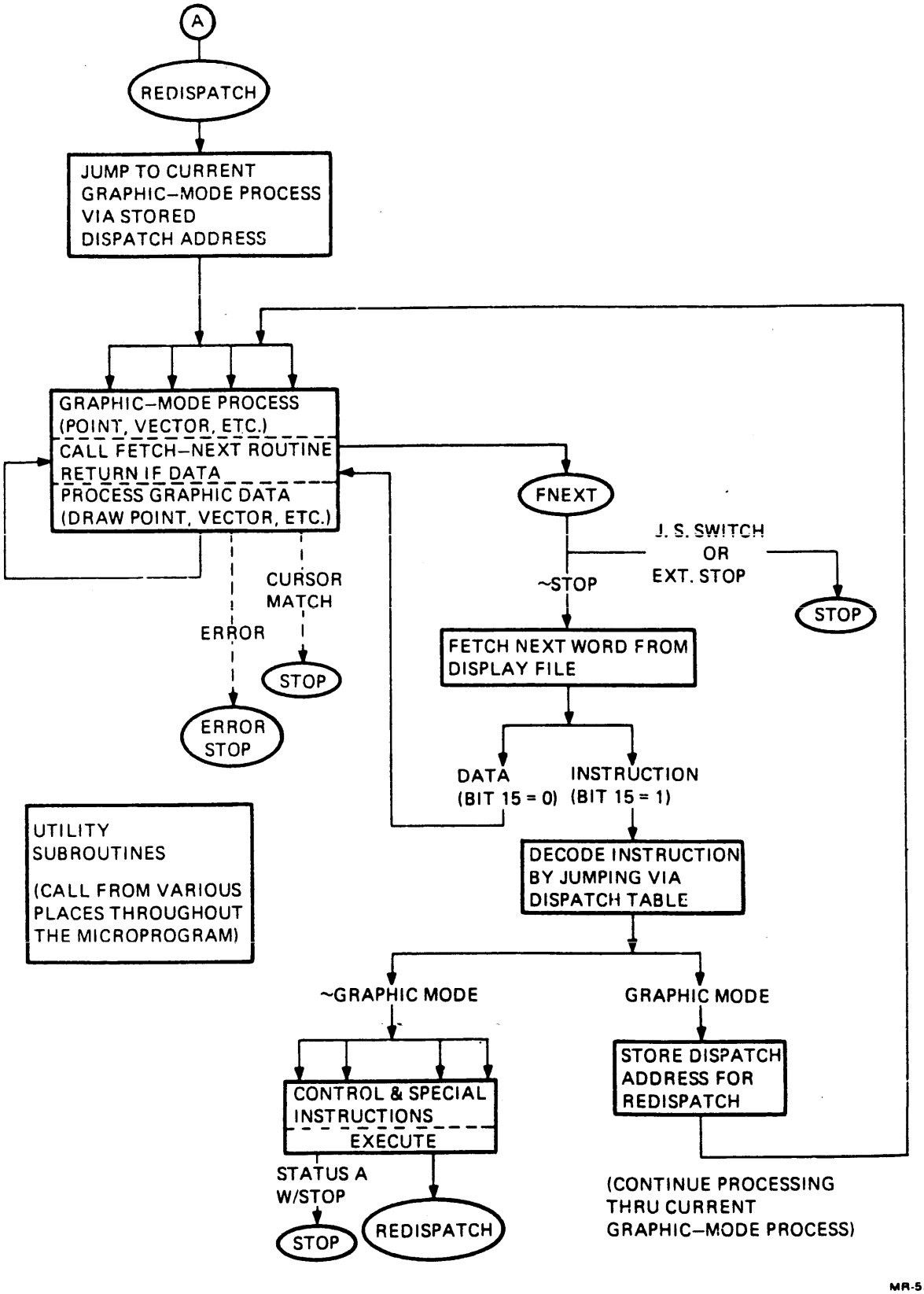


Figure 4-13
Microprogram Overview (Sheet 2 of 2)

CHAPTER 5

M7062 IMAGE MEMORY TECHNICAL DESCRIPTION

5.1 INTRODUCTION

The M7062 Image Memory module (M7062) contains thirty-two 16K X 1-bit Random Access Memories (RAMs) for storing data to be displayed on the video screen. Up to 16 colors of red, green, and blue combinations, or 16 shades of grey (intensity levels), can be stored in memory. The M7062 is the memory module for the VSV11/VS11 Graphic System. The M7062 receives its timing from the Sync Generator/Cursor Control module (M7061) via the backplane Video Bus (VBUS) and it receives data from the Display Processor (M7064) via the daisy-chained Data Bus (DBUS) cable. When requested, the data stored in the M7062 is sent to the digital-to-analog circuits (DACs) in the Sync Generator module to provide the composite video out.

5.2 GENERAL DESCRIPTION

The M7062 memory resembles a Cartesian coordinate system; that is, video data is stored in a specific X-Y address. Data is normally being read out of memory as the display scan proceeds across the video screen. Horizontal and Vertical counters keep track of the scan position (address). These counters receive their clock and load signals from the Sync Generator module, as shown in Figure 5-1. The horizontal and vertical position of the scan is presented to the Read/Write Multiplexer which presents this address to the memory. The data in memory at that address is loaded into a Shift Register, then into a latch, to become video data out.

The load register signals, the write request, and data are received from the Display Processor via the Data Bus (DBUS). This bus is a 40-conductor ribbon cable that connects to the Berg connector on each M7062 module in the system. The D Select Multiplexer decodes the load register signals from the Display Processor. One of these load signals is used to select the mode. The modes used most often enable the write logic (Mode W, allowing the Display Processor to write into the memory) and/or the read logic (Mode R, causing the data stored in memory to be read out to the monitor via the DAC on the M7061 module).

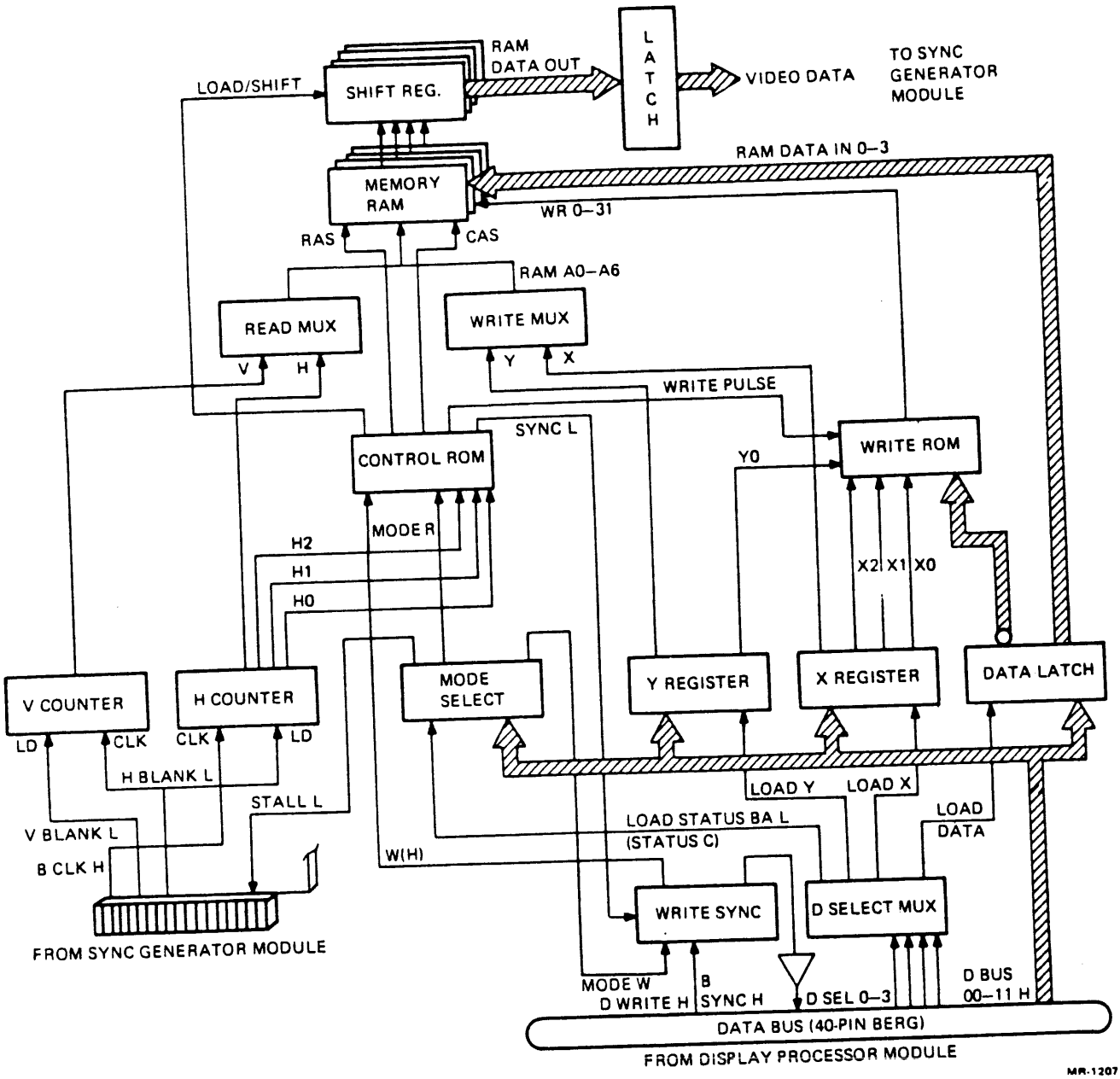


Figure 5-1
M7062 Image Memory Block Diagram

When a write to memory is desired, the data (color/intensity) is loaded into the Data Latch. This can be data for a point, series of points (vector), graph, histogram, etc. The address is then loaded into the X and Y Registers. This can be done at any time as the data is not written into memory until a WRITE signal comes from the Display Processor. The signal, in conjunction with a Write Sync condition, allows a write pulse to the Write ROMs. The Horizontal and Vertical Counters are disabled at this time, and the address information comes from the X and Y Registers. When the WRITE signal is removed by the Display Processor, the Read/Write Multiplexer once again gets its address information from the Horizontal and Vertical Counters.

The Control ROM is the main timing generator within the M7062. It uses the system clock from the Sync Generator module and the three least-significant bits from the Horizontal Counter as 8 time states to create the timing signals. One of its outputs is a SYNC pulse to synchronize a write to memory from the Display Processor. The Control ROM also controls the Read/Write Multiplexer, the Write ROM, and the Shift Registers.

The M7062 has the following configuration considerations (refer to Chapter 2 for configuration and setup details):

- Each M7062 is switch selectable as a 512 X 512 X 2 Interlaced memory, or a 512 X 256 X 4 Non-Interlaced memory.

- Each M7062 accepts either 2 or 4 of 8 switch selectable data input lines from the Data Bus (D BUS <09:02>).

- Each M7062 transmits either 2 or 4 video data bits to the DACs in the Sync Generator module selecting from eight video output data lines to the Video Bus (V DATA <7:0>).

- Up to four M7062s, configured in two groups of 4-bit memories, can be installed in a dynamic configuration using one Sync Generator module.

- All M7062 modules must be configured as either Interlaced or Non-Interlaced to match the configuration of the Sync Generator module.

5.3 SYSTEM CLOCK

The system clock for the M7062 is generated by the M7061 Sync Generator module. This is a 12.6 MHz clock (B CLK) from the Video Bus, as shown in Figure 5-1. B CLK L is received from the Video Bus and inverted to SYS CLK H for the M7062. This clock is directly or indirectly used by the Horizontal Counter, the RAM memories, Shift Registers, and the Video Output Latch. With this clock, video is displayed for all 512 horizontal locations in memory, as shown in Figure 5-2.

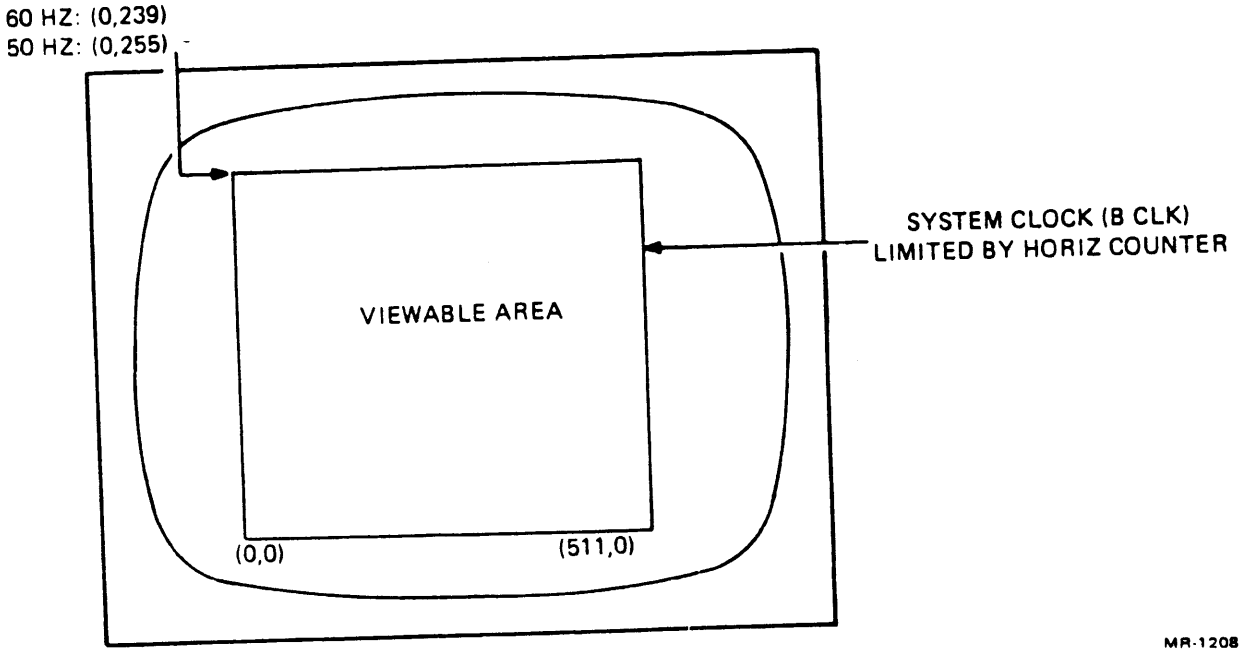


Figure 5-2
Viewable Area of Video Screen

5.4 HORIZONTAL AND VERTICAL COUNTERS

The Horizontal and Vertical Counters keep track of the X and Y address of the video scan. The Vertical Counter is loaded by the V BLANK L signal from the Sync Generator module. At 60 Hz this counter is loaded to 240. At 50 Hz it is loaded to zero; this represents a count of 256. The Vertical Counter counts down from these values after each scan when H BLANK L goes high.

SYS CLK H (Figure 5-3) synchronizes the H BLANK L signal and provides a CLEAR signal, at the same time, to the Horizontal Counter. The Horizontal Counter counts up with each SYS CLK H pulse.

D MEM CLK L, from the M7064 Display Processor, is clocked into the H0 bit of the Horizontal Counter with SYS CLK H signal to ensure that the M7062 and the M7064 are in phase before starting to count.

The C OUT X (Carry Out of X) signal disables reading out of memory after the Horizontal Counter counts up to 512. The CLR X L signal clears this condition and allows reading from memory

after the Horizontal Counter has been reset to zero.

The three least significant bits of the Horizontal Counter are sent to the Control ROM to generate 8 time states within the ROM. The remainder of the outputs from the Horizontal and Vertical Counters are sent to the Read/Write Multiplexer, as address information, while reading from memory.

During a memory clear operation, the Horizontal and Vertical Counters are used to access all memory locations so they can be cleared to zero or some other data value. Only active screen lines are cleared by the CLR function.

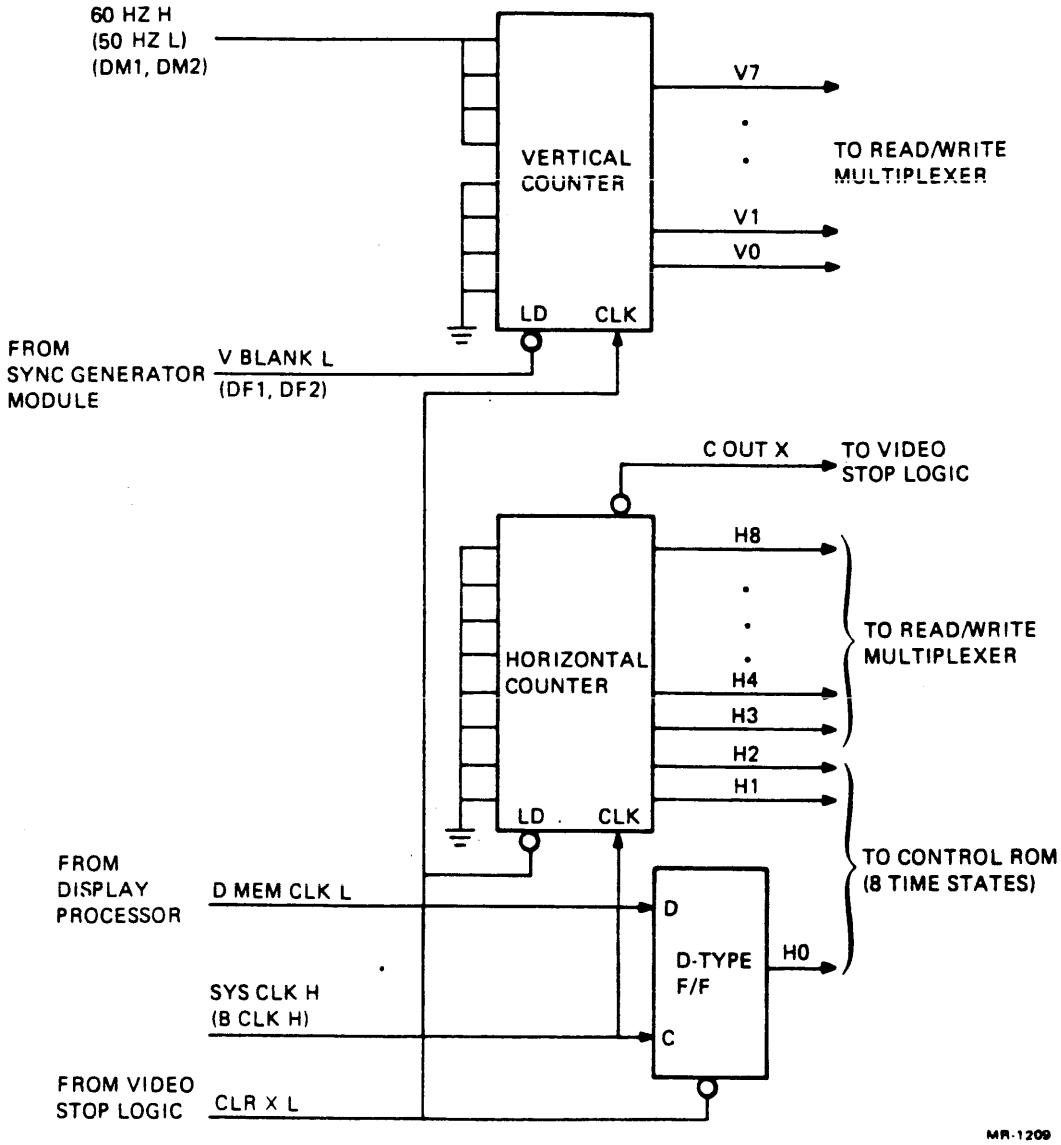


Figure 5-3
Horizontal and Vertical Counters

5.5 READ/WRITE MULTIPLEXER

The Read/Write Multiplexer takes the horizontal and vertical address information and alternately transfers this information to the RAM memories. As illustrated in Figure 5-4, each multiplexer has a "select (SEL)" input and an "output enable (OE)" input. The row or column select signal alternately selects the X ADDRESS "B" then the Y ADDRESS "A" inputs; that is, the HORIZONTAL ADDRESS "B" then the VERTICAL ADDRESS "A". The output enable signal, ENABLE READ L, selects which multiplexer is in operation. During a read, the RAM address is received from the Horizontal and Vertical Counters; during a write, from the X and Y Registers. The output address, RAM A0--RAM A6, is sent directly to the RAM memories.

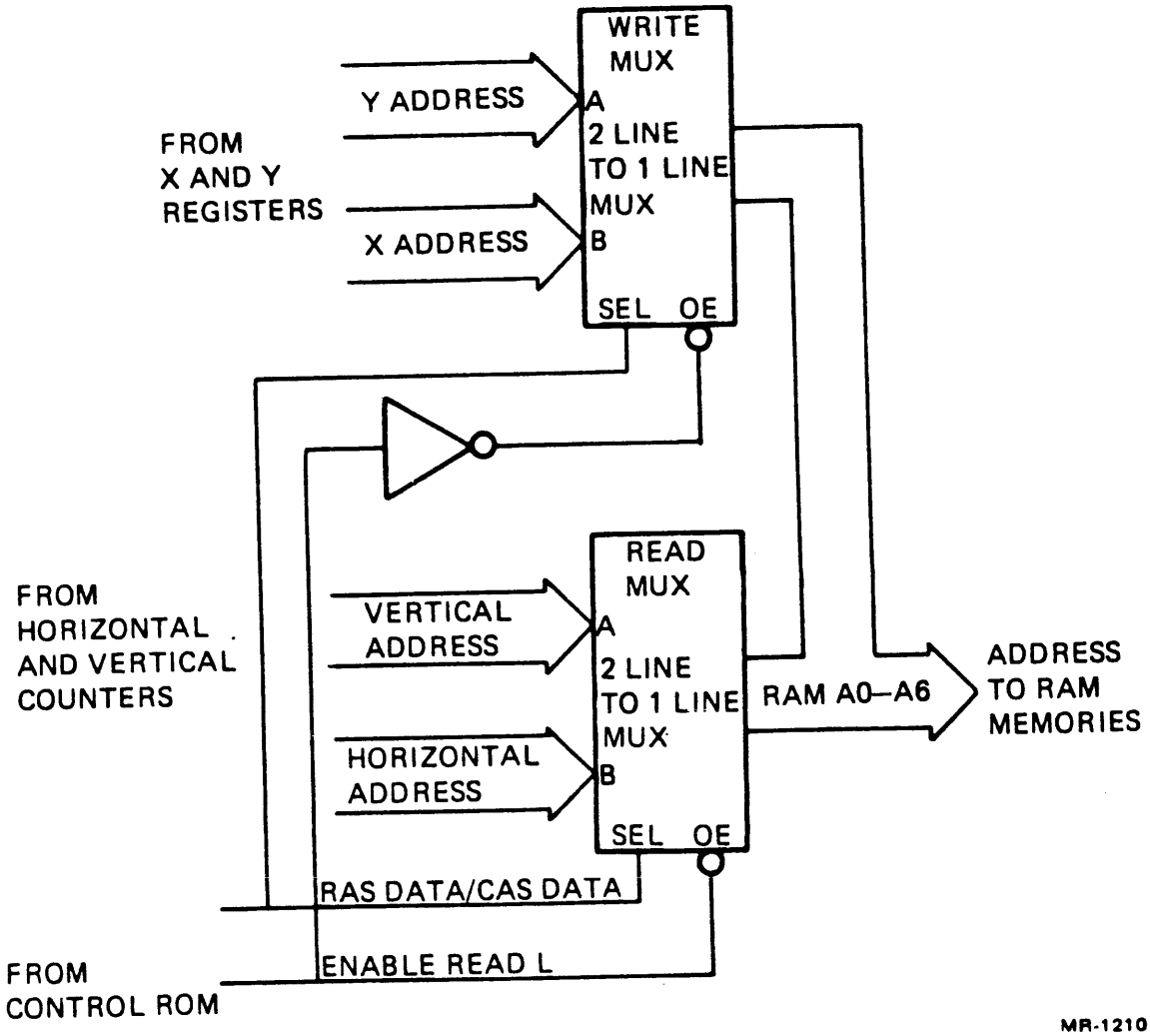


Figure 5-4
Read/Write Multiplexer

5.6 RAS AND CAS MEMORY ADDRESS

Row Address Strobe (RAS) and Column Address Strobe (CAS) are two enable pulses to alternately clock the row and column address of the video scan position into memory. During a read operation, this address comes from the Horizontal and Vertical Counters; during a write operation, from the X and Y Registers. The sources of the RAS and CAS addresses are as shown in Figure 5-5.

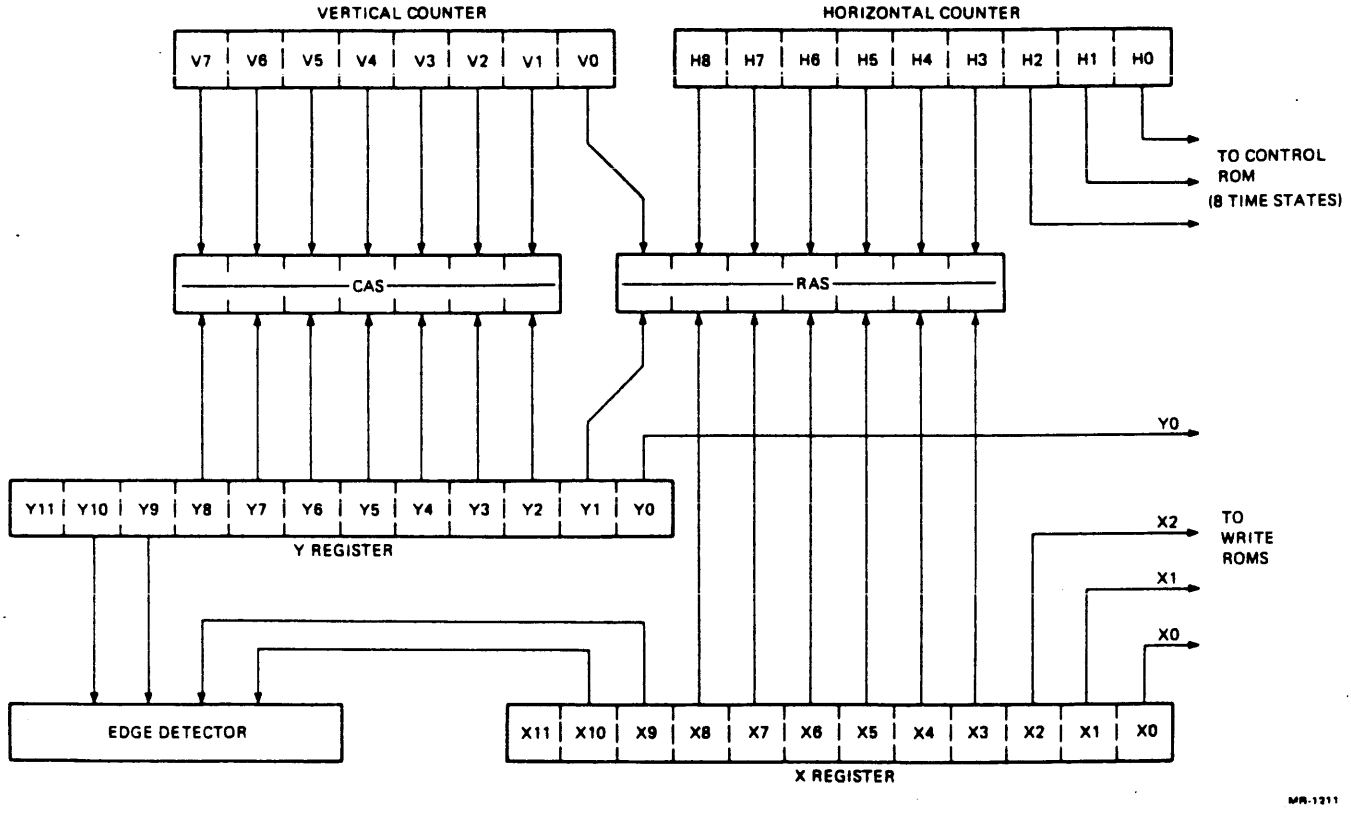


Figure 5-5
RAS and CAS Memory Address

5.7 MEMORY AND SHIFT REGISTER

The M7062 memory consists of thirty-two 16K X 1-bit Random Access Memory (RAM) integrated circuits as shown in Figure 5-6. The memory is switch selectable as either 512 X 256 X 4 bits or 512 X 2 bits. Each memory chip uses the RAM ADDRESS lines and the RAS (row) and CAS (column) address strobe inputs. Each memory chip has its own write input. The memory data, RAM DATA IN, supplied by the Data Latch, represents up to 16 possible combinations of color or intensity levels.

As the memory is accessed by the row and column address, the data in memory is presented to one of eight parallel inputs to a Shift Register. When the LOAD/SHIFT input is low, the data is loaded into the shift register and when high, the data is shifted by the B CLK LATCH pulse which is a function of the SYS CLK. It takes eight clock pulses to completely shift out the data from the 8 parallel RAMs.

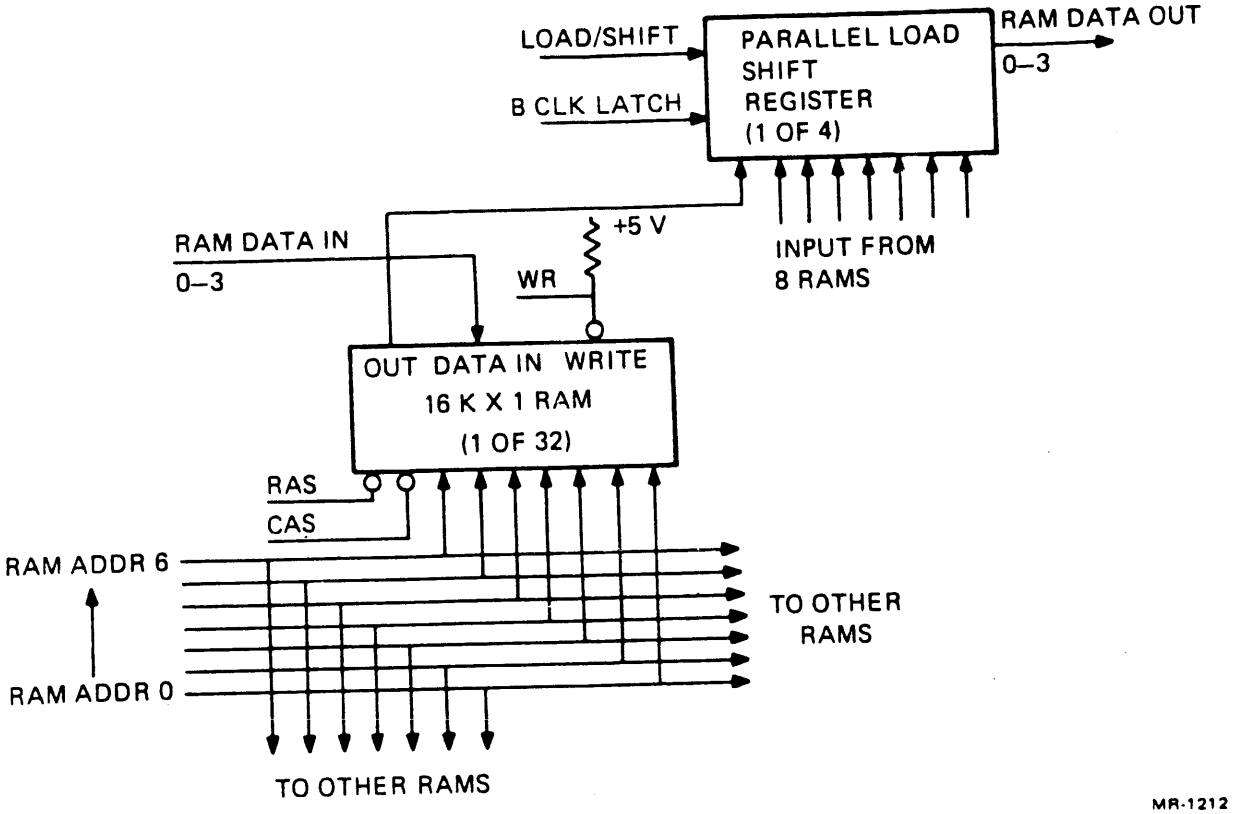


Figure 5-6
Memory and Shift Register

5.8 VIDEO DATA OUT

The data from the four memory Shift Registers (RAM DATA OUT) is clocked into a latch. This data goes through a switch pack to the Video Bus, as shown in Figure 5-7. These switches set up the number of bits deep of memory (either 2 or 4) for Interlaced or Non-Interlaced mode. They also determine which data lines are selected as inputs to the DACs in the Sync Generator module. Refer to Chapter 2 for the configuration of these switches to enable the desired output.

During Interlaced mode, the signal OUT HI BYTE H (from the Interlace ROM) is low for half the system clock time, disabling the upper two data bits. When this happens, the signal OUT LO BYTE H is high and enables the lower two data bits from memory to be placed on the Video Bus. When the signals change state, the upper two data bits from memory are enabled and are placed on the same V DATA lines of the Video Bus.

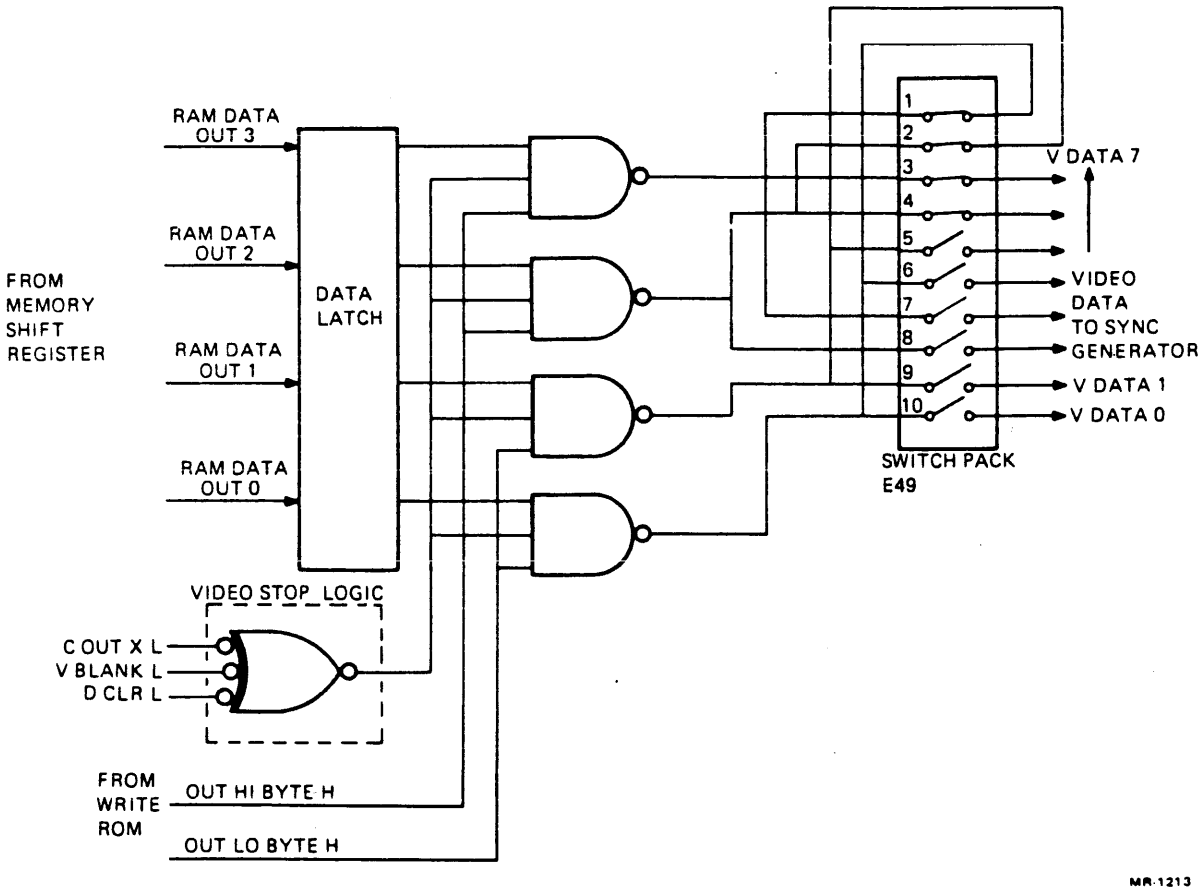


Figure 5-7
Video Data Out

During Non-Interlaced mode, the signals OUT HI BYTE H and OUT LO BYTE H are always high, enabling data onto four V DATA lines of the Video Bus.

Video output is disabled during video blank time or after the Horizontal Counter has reached a count of 512 creating the C OUT X L signal. The video output is also disabled during D CLR L (from a Clear instruction).

5.9 DATA BUS (DBUS)

The M7062 receives its display data and control signals via the Data Bus. This bus is a 40-conductor ribbon cable connected from the Display Processor module, to each Memory module and each Sync Generator module. Signals on this bus include the following:

1. D BUS data lines (12 lines): X, Y image coordinate address; data for writing into memory; and mode select or status information (D BUS <11:00>).

2. Data Select lines (4 lines): D SEL <03:00> provide up to 16 binary coded signals for controlling data transfers and loading the registers.

3. Write Control lines (2 lines): Lines to control the timing of data transfers across the Data Bus (B SYNC L from the M7062 and D WRITE H to the M7062).

4. Clear line (1 line): D CLR L clears all write-enabled M7062 modules installed on the bus.

5. Pixel Read-back lines (2 lines): These lines control reading data back from memory (to the Display Processor) at specific pixel locations (D RQST DATA L and DATA AVAIL L).

6. Cursor Interrupt lines (2 lines): A Joystick Switch interrupt and a Cursor Match interrupt; these lines are not used by the M7062.

The M7062 uses 3-state drivers to drive B RAM DATA 03-00 onto the Data Bus to return requested data back to the Display Processor during pixel readback.

5.10 D SELECT MULTIPLEXER (DECODER)

The select input signals from the Display Processor, D SEL 00, 01, and 02, are decoded by a 3-line-to-8-line Multiplexer, as shown in Figure 5-8. The signals D SEL 03 and D PULSE 00 are enable signals. The multiplexer outputs, listed in Table 5-1, are mutually exclusive. Only one output is enabled when the Display Processor issues the D PULSE 00 L signal. These outputs enable data to be loaded from the Display Processor into the X and Y Address Registers, the Data Latch, or the Mode Select (STATUS BA) Logic. The LOAD STATUS BA function must be enabled by the correct memory channel address, appearing on DBUS bits 11 and 12.

The SWITCH L signal allows read/write switch selection between memory channels for implementing dynamic (moving) displays. This signal facilitates handling a read from one M7062 memory while altering data in another M7062. Upon the command SWITCH, the role of each memory is interchanged, and video data is taken from the memory with the new data.

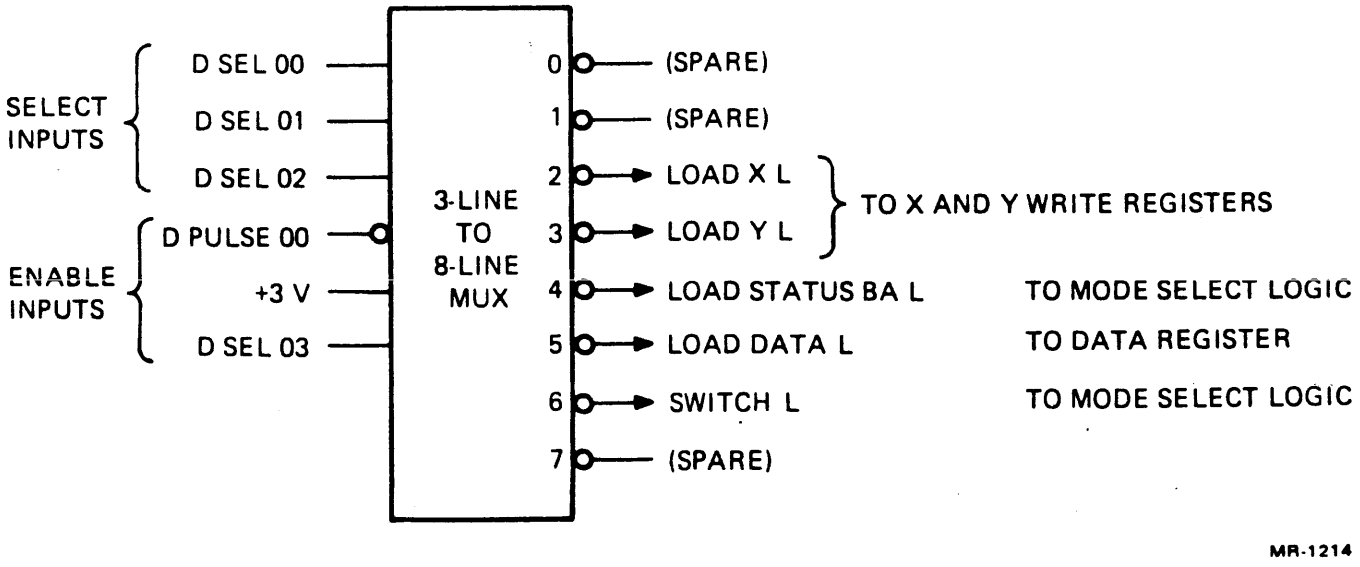


Figure 5-8
D Select Multiplexer (Decoder)

Table 5-1
D Select Multiplexer Functions

Enable D SEL 03	Select Inputs D SEL 02	01	00	Output Function
H	X	X	X	None (All Outputs Disabled)
L	L	L	L	Spare (not used)
L	L	L	H	Spare (not used)
L	L	H	L	LOAD X L
L	L	H	H	LOAD Y L
L	H	L	L	LOAD STATUS BA L (Status C)
L	H	L	H	LOAD DATA L
L	H	H	L	SWITCH L
L	H	H	H	Spare (not used)

5.11 DATA LATCH

When a write to memory is desired, data is loaded into the Data Latch, shown in Figure 5-9. This data comes from the Display Processor via the Data Bus. Depending on whether the M7062 is set up for an Interlaced or a Non-Interlaced mode, this data may be either 2 or 4 bits and may represent up to 16 colors or intensity variations. The switch pack is set to accept the desired Data Bus lines in the selected mode. Refer to Chapter 2 for proper switch selection.

The data may be loaded into this latch at any time. It is held here until another LOAD DATA pulse comes along. The data may also stay in the Data Latch for a series of "X, Y" locations which may represent a vector, shading a graph, or clearing the memory to a specific data value (or color).

The signal CLR H will clear all M7062 modules that are write enabled. It will force all zeros into memory as long as D BUS 05 is high. If D BUS 05 is low, CLR H will clear all memory to the data stored in the Data Latch; this may be one specific color, such as green, or one intensity. The Display Processor will generate a clear sequence during its initializing routine after setting all M7062 modules to the write mode. Refer to Paragraph 5.16.

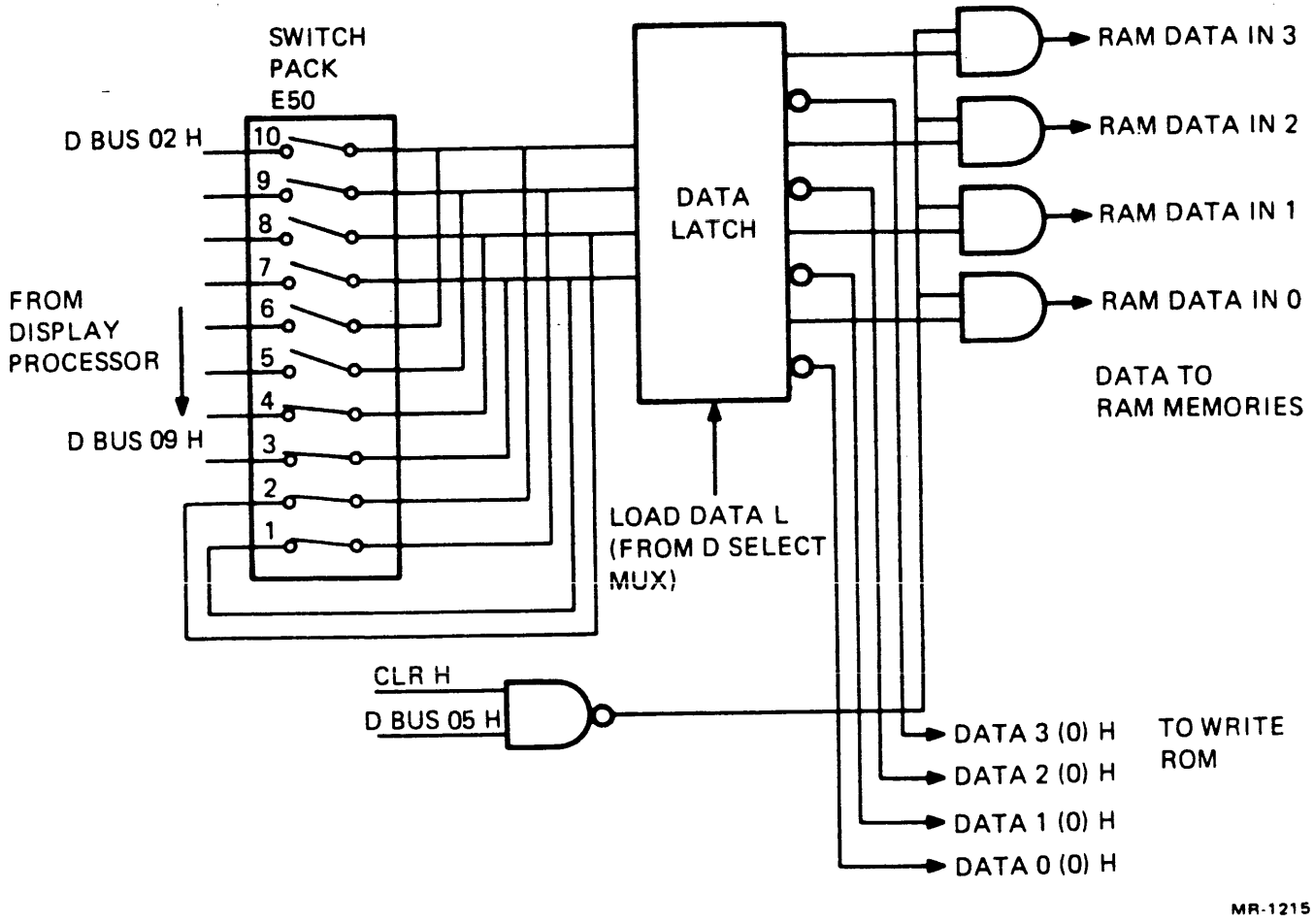


Figure 5-9
Data Latch
(Shown in Interlaced Mode for D BUS 08, 09)

5.12 X AND Y REGISTERS

The address for the data to be written into memory is loaded into the X and Y Registers, shown in Figure 5-10. The address is loaded with a low-to-high transition of the LOAD X, or LOAD Y, pulse from the D-Select Multiplexer. This address is presented to the Read/Write Multiplexer, but it is only enabled to memory during a write cycle.

Address lines in excess of the viewable area of the video screen are sent to an edge detector to prevent wraparound; for example, if the Display Processor is calculating the vectors of the triangle shown in Figure 5-11a, the upper portion of the triangle would not be displayed, since they would appear as extraneous lines on the video screen, as in Figure 5-11b.

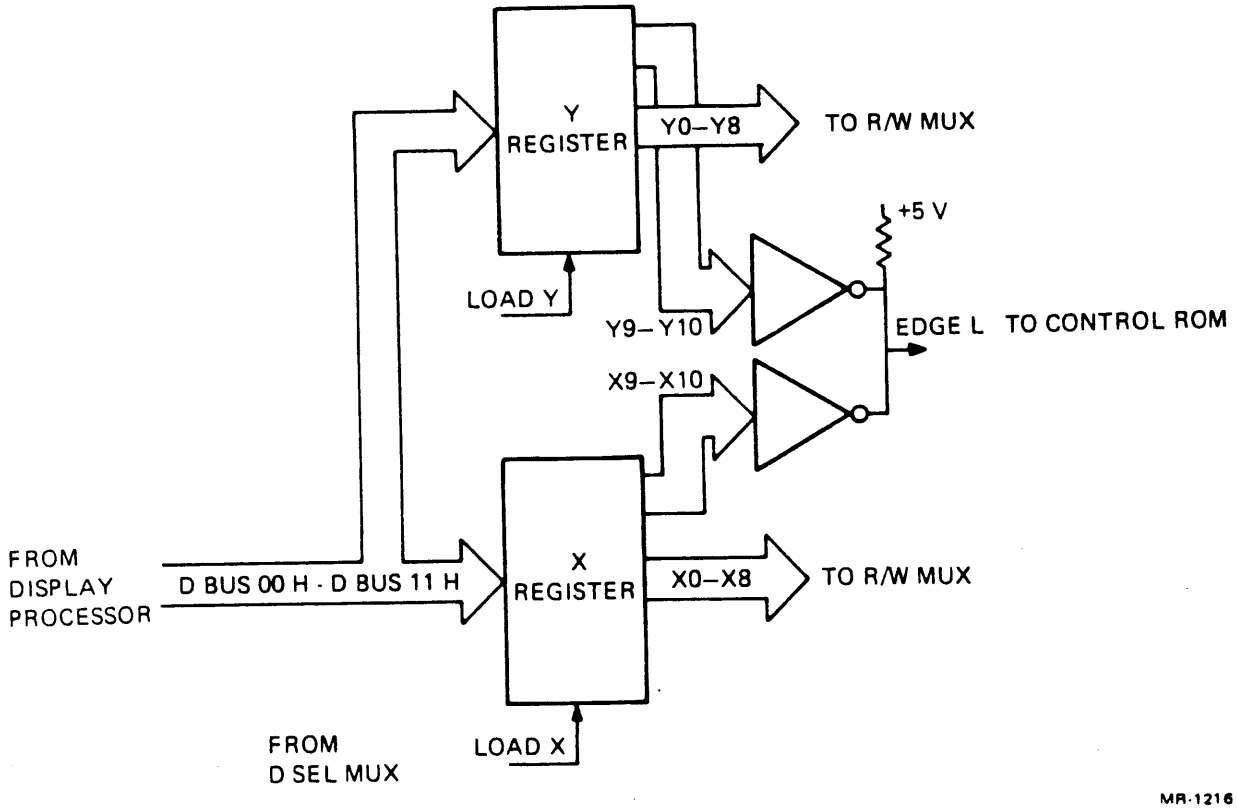


Figure 5-10
X and Y Registers

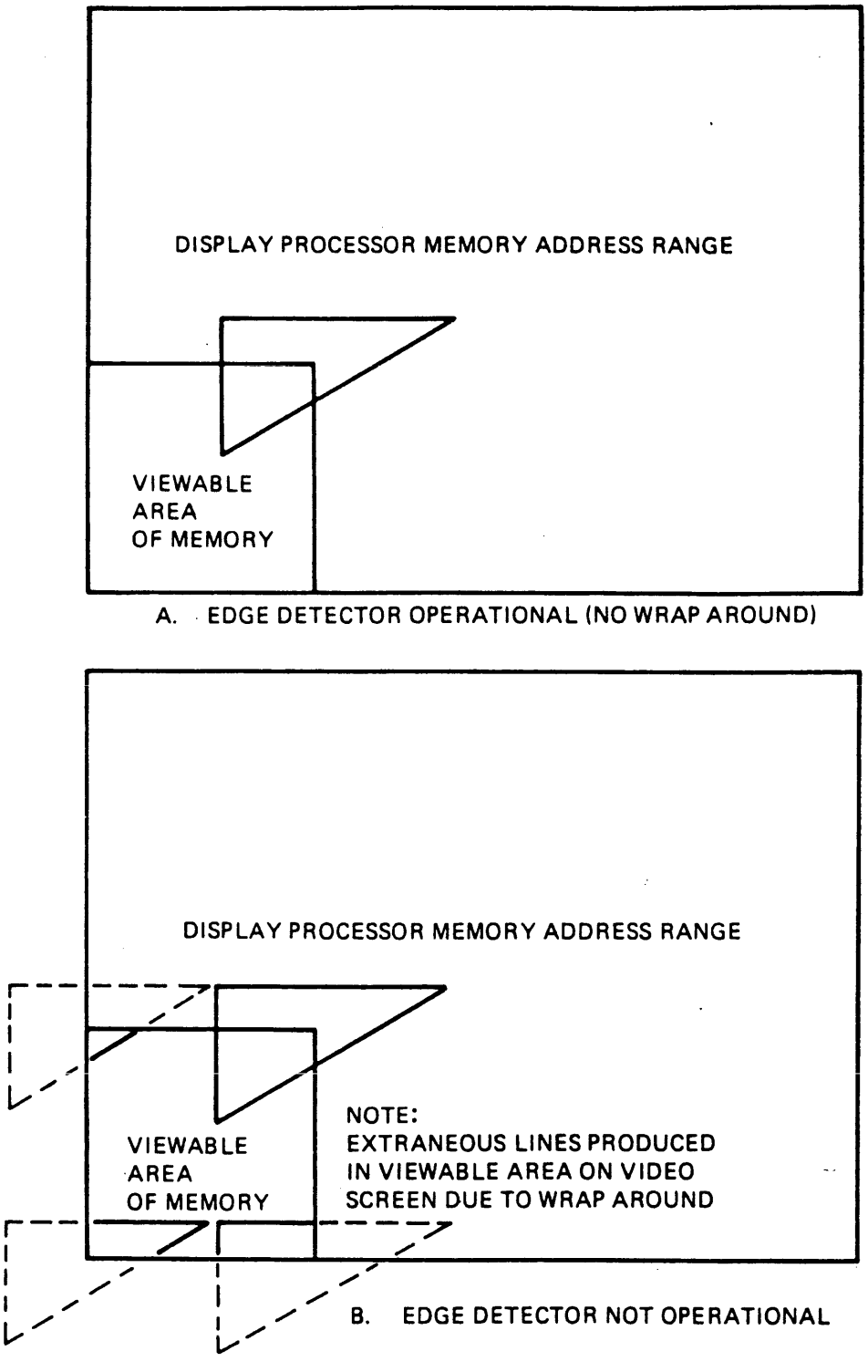


Figure 5-11
Edge Detector Operation

5.13 WRITE ROM

The lower 3 bits of the X Register are the address input bits of each Write ROM, as shown in Figure 5-12. These 3 bits select one of eight memory RAMs in each of four groups of memory chips. The Interlace ROM detects if the Sync Generator module is in Interlaced or Non-Interlaced mode. During Non-Interlaced mode, all four Write ROMs are strobed at the same time by the signal WR PULSE L; for example:

> WR00, WR08, WR16, and WR24 are enabled (low) if X0, X1, and X2 equal zero.

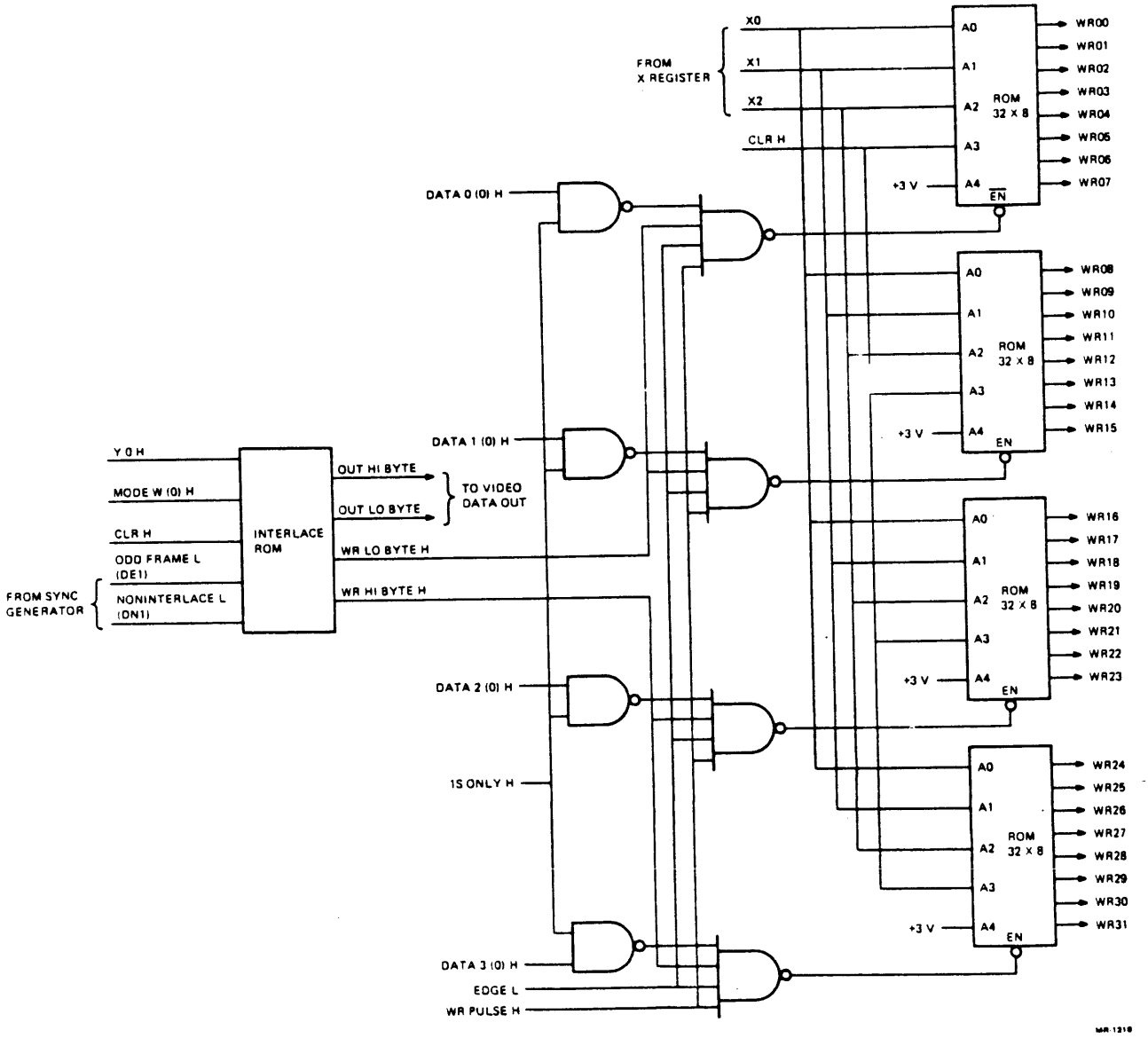


Figure 5-12
Write ROM

During Interlaced mode, only two Write ROMs are strobed at a time. Selection is controlled by the least-significant bit of the Y Register (Y0). When Y0 is low, the lower two Write ROMs are strobed; when Y0 is high, the upper two ROMs are strobed; for example:

> With X0, X1 and X2 equal to 0, WR00 and WR08 are enabled when Y0, is low; WR16 and WR24 are enabled when Y0 is high.

The clear signal, CLR H, will force a low write pulse from each write output, WR00 through WR31, to clear the memory to all zeros (or to the data in the Data Latch, as explained in Paragraph 5.11). As the Read/Write Multiplexer addresses the memory, it is cleared by writing zeros (or a specific data value) into each memory location.

The output of the Write ROM can be disabled if a zero is being written under the control of the 1S ONLY H signal. This signal is enabled by the Mode Select (STATUS BA) logic. With 1S ONLY H present, a NAND gate at each Write ROM monitors the data in the Data Latch to be written into memory. If the data bit is a one, the Write ROM to that location in memory is enabled. If the data bit is a zero, the Write ROM is disabled, and the write pulse does not allow that zero to be written into memory; the data in memory at that location will remain unchanged.

When drawing lines on the video screen with different intensities, this allows the line with the higher intensity to be dominant. Without enabling 1S ONLY H, a line of lower intensity drawn over a line of higher intensity will cause an apparent break in the high intensity line at the crossover point. Examples with 1S ONLY H enabled follow:

	Intensity of 1st line	Intensity of 2nd line	Intensity at Crossover Point
Example 1:	0001	0111	0111
Example 2:	0101	0110	0111

5.14 WRITE SYNCHRONIZATION LOGIC

For a memory write, MODE W is enabled from the Mode Select Logic. The Display Processor issues a D WRITE H signal to the M7062 and waits for a synchronization signal (B SYNC L) before sending X and Y data to the memory as shown in Figure 5-13.

Both Mode W (write) and Mode R (read) can be enabled at the same time. Memory is then written only during retrace time. When both modes are enabled, writing is controlled by ENA WRITE L from

the Video Stop logic. As the Horizontal Counter increments, data is read from memory, ENA WRITE L is high, and B SYNC L is disabled. No writing occurs at this time. After the row of data has been read, ENA WRITE L goes low, B SYNC L reaches the Display Processor, and writing occurs during retrace time.

Every 30 lines the memory is refreshed by the REFRESH L signal from the Sync Generator module. This signal is ignored while Mode R is enabled, since reading the dynamic RAMs at the video frame rate also refreshes them; however, refresh is necessary while Mode R is zero (i.e., while the memory is in Write-Only or Protect mode) to keep from losing data.

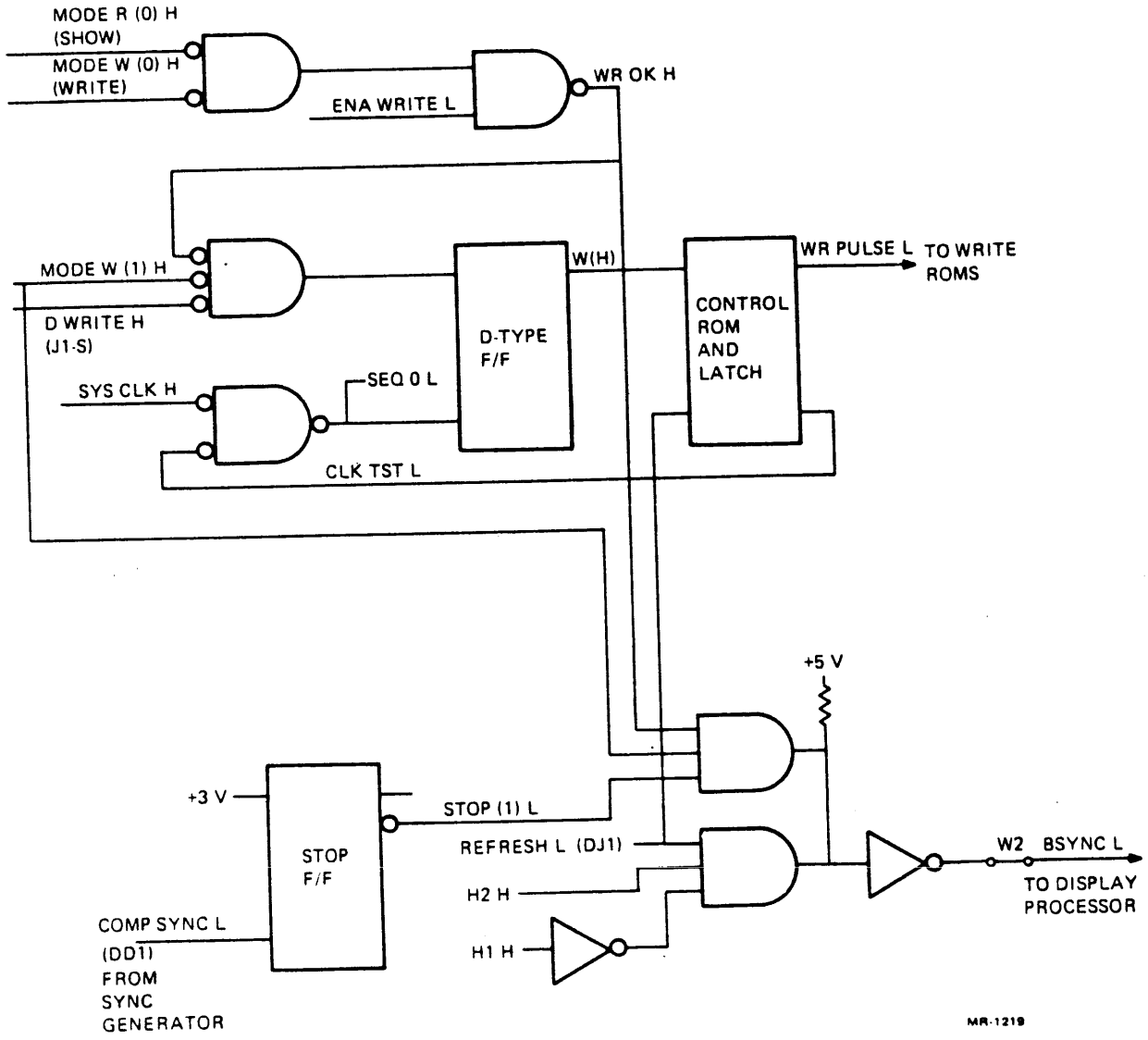


Figure 5-13
Write Synchronization Logic

The Refresh signal is held low for two line times, during which the M7062 completes its operation on the current line, then memory is refreshed. B SYNC L is disabled during refresh time so the Display Processor stops sending data while the memory is being refreshed.

The synchronization signal need be enabled on only one M7062 in each memory channel. Jumper W2 can be removed from all other M7062 modules used in that channel. B SYNC is issued only during states four and five of the eight state memory timing cycle (Paragraph 5.17).

5.15 VIDEO STOP LOGIC

When the Horizontal Counter reaches a count of 512, it provides the C OUT X L signal that sets the Horizontal Detect flip-flop (Figure 5-14). This is clocked into the Video Stop latch, which disables the video output gates. Likewise, the Clear instruction from the Display Processor (D CLR L) disables the video output while clearing the memory. This operation is synchronized by the D REQ DATA LAT H signal from the Control ROM circuit.

When the video output is disabled, ENA WRITE L allows writing into memory during retrace time when both the Read and Write modes are enabled at the same time. This eliminates disruption of data on the screen.

When the negation of H BLANK L resets the Stop and Clear flip-flops, CLR X (1) clears the Horizontal Detect flip-flop to allow video output.

MEM STOP L synchronizes the Control ROM so that the current read or write operation is finished before clearing the RAMs.

CLR X L is used to reset the Horizontal Counters and clock the Vertical Counters.

5.16 MODE SELECT LOGIC (LOAD STATUS BA)

DBUS Data bits 11 and 10 determine if the signal LOAD STATUS BA L will be enabled on this M7062 module. Up to four M7062 modules are address selectable in a VSV11/VS11 Graphics System by using jumpers, as shown in Figure 5-15. The state of D BUS 11 and D BUS 10 determine the channel selected; refer to Chapter 2 for channel selection.

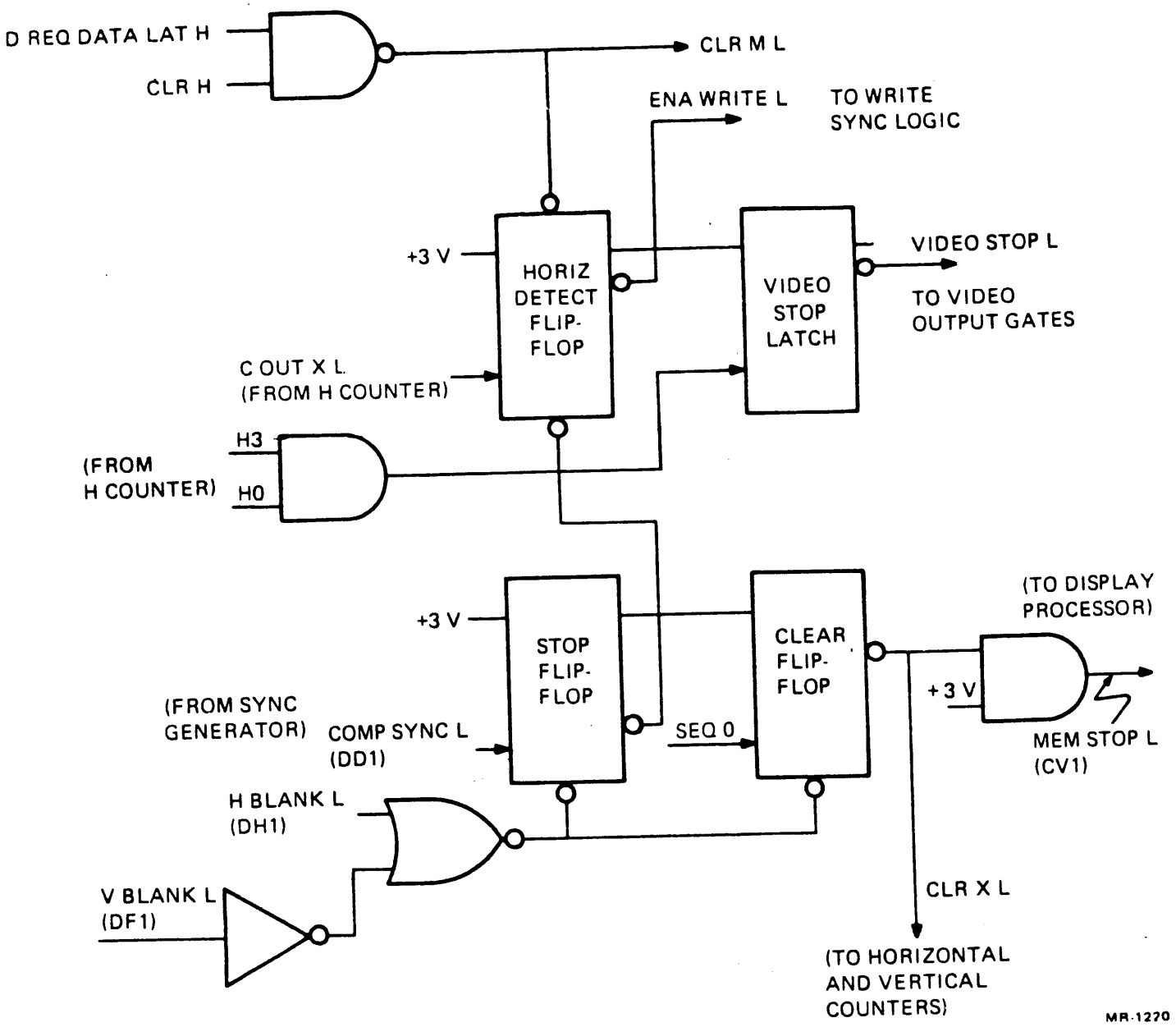


Figure 5-14
Video Stop Logic

D BUS 07 should be set to zero. This allows LOAD STATUS BA L to load the Mode Select logic with D BUS 00 through 05.

D BUS 01 H and D BUS 02 H are used to load the 1S ONLY H signal, which allows writing only ones into memory. This signal is used by the write logic to draw lines of variable intensity over one another without leaving an apparent gap in either line (Paragraph 5.13).

D BUS 03 H is used to enable the SWITCH L signal (from the D Select Multiplexer) to toggle two memory sets between Write and Read modes to obtain dynamics.

D BUS 04 H is used to set Mode W, the "write into memory" mode.

D BUS 05 H sets Mode R, the "display memory" (read) mode.

NOTE

Status bits 04 and 05 must be cleared on the M7062 to write-protect the memory data. During the Display Processor's initializing routine, all memory channels are set to write mode and cleared with the C CLR L signal.

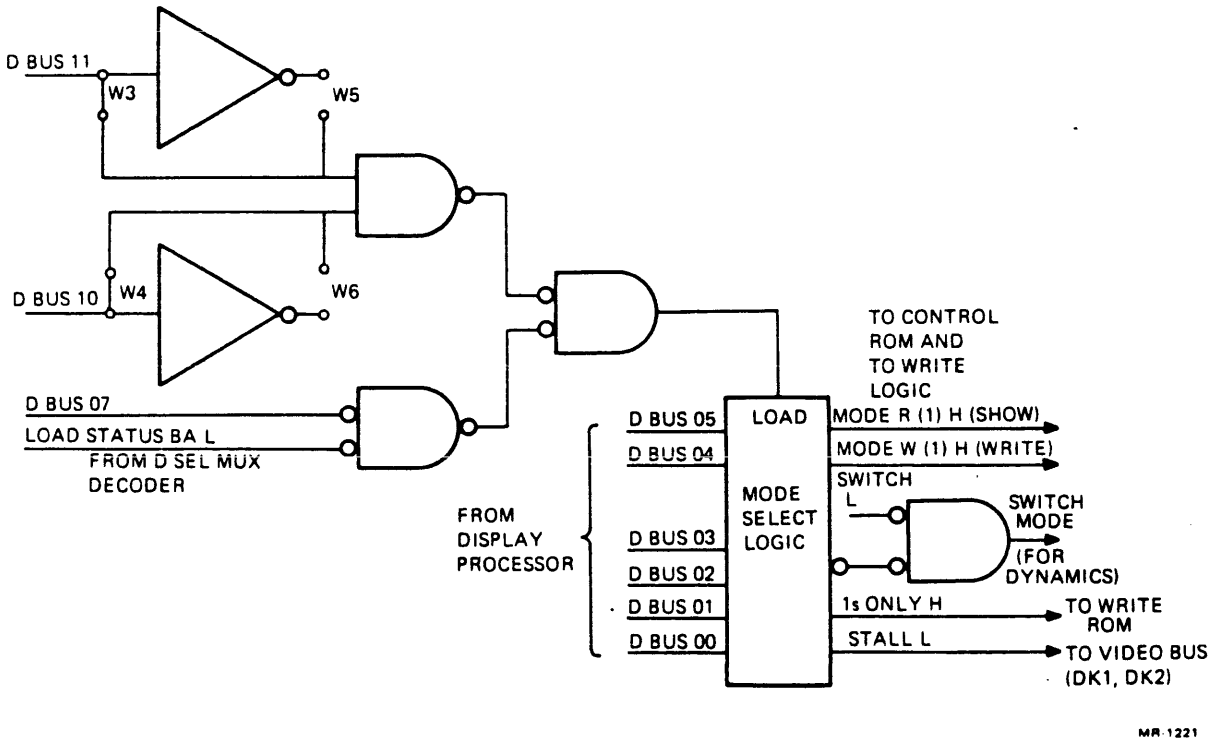


Figure 5-15
Mode Select Logic

5.17 CONTROL ROM AND TIMING

The Control ROM, a 256 X 8-bit Read Only Memory, and its associated latch form the main timing controller for the M7062. Each input, shown in Figure 5-16, and its function is described below:

1. H0, H1, H2: These three signals, the lower 3 bits of the Horizontal Counter, are used to generate 8 time states within this ROM.

2. W(H): This is the write signal formed by D WRITE H from the Display Processor and enabled by the write mode, Mode W. It synchronizes the memory to the Display Processor, generates the output WRITE PULSE H, and allows the ROM to switch to the X and Y Registers for address information.

3. C(H): The signal D CLR L from the Display Processor, when enabled by the write mode, creates the C(H) signal to the Control ROM. This enables the WRITE PULSE L and uses the Horizontal and Vertical Counters to quickly clear the memory.

4. MODE R (1) H: This is the read mode that generates the ENA READ L signal to the Read/Write Multiplexer and provides the LOAD L/SHIFT H signals to the RAM Memory Shift Registers. If not enabled, only zeros will be shifted out of the shift registers.

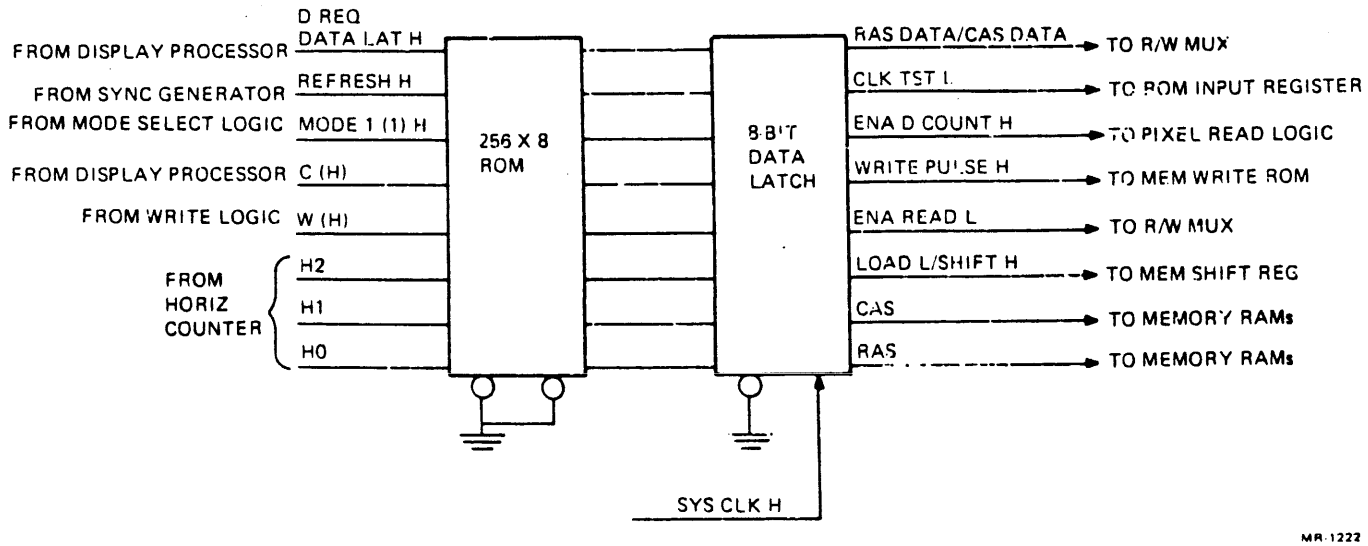


Figure 5-16
Control ROM

5. REFRESH H: This signal from the Sync Generator module is generated for every 30 lines to refresh the memory. The refresh signal is held for two line times, during which writing on the current line is completed before the entire memory is refreshed.

6. D REQ DATA: This is a pixel read back request signal from the Display Processor to request data from a specific memory location (addressed by the X and Y Registers). For example, it is used in diagnostics to compare data in memory to an expected value.

The timing diagram for the output signals from the Control ROM is shown in Figure 5-17. These signals and their functions are as follows:

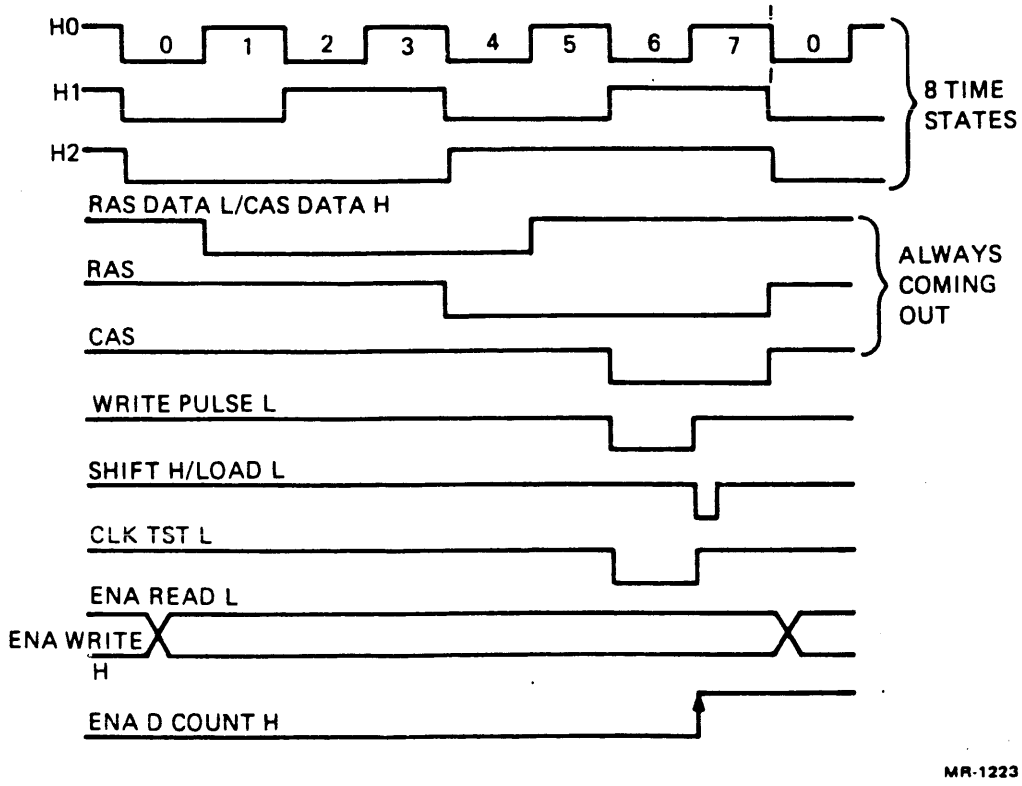


Figure 5-17
Control ROM Timing Diagram

1. RAS and CAS: Row Address Strobe and Column Address Strobe are used to load the address information from the Read/Write Multiplexer into the RAMs.

2. LOAD L/SHIFT H: This signal loads parallel data from 8 memory RAMs into the shift register, then it shifts the video data out with 8 clock pulses.

3. ENA READ L: When present this signal enables the Read/Write Multiplexer to get address information from the Horizontal and Vertical Counters. When disabled, the multiplexer gets address information from the X and Y Registers.

4. WRITE PULSE H: This is a timed strobe that is used to enable input to the Write ROM. This signal is gated by EDGE L in the Write ROM enabling circuits if the Display Processor is calculating data outside the video display area (Paragraph 5.12).

5. ENA D COUNT H: This is a pixel read-back signal used to read data stored in memory back to the Display Processor.

6. CLK TST L: This signal synchronizes any changes to the Control ROM by enabling the clock input of the ROM input register.

7. RAS DATA/CAS DATA: This signal controls the Read/Write Multiplexer. It alternately selects horizontal, then vertical, data during a read mode; or t selects X data, then Y data, during a write mode.

The B SYNC L signal sent to the Display Processor is a function of the H2 and H1 Horizontal Counter bits. The B SYNC L signal is issued only during time states four and five. The signal allows the Display Processor to synchronize with the memory timing so that a new X address is sent during time states zero and one. A new Y address is sent during time states two and three. If new Pixel Data is required, it is sent during time states four and five.

5.18 PIXEL READ-BACK LOGIC

The M7062 has a pixel read-back mode that allows the Display Processor to read a specific location from memory in the M7062. It first loads a coordinate position into the X and Y Registers, then it sends the D REQ Data L and the D WRITE H signals. The WRITE pulse synchronizes the position; D REQ DATA L indicates to the M7062 not to write data, but rather read data from that position back to the Display Processor. Pixel Readback is enabled by Mode W (i.e., the memory must be in Write-Only or Read/Write mode).

The Control ROM in the M7062 then enables the ENA D COUNT LAT H signal to strobe the lower 3 positions of the X Register into a down-counter as shown in Figure 5-18. When this counter gets to

the desired location (1 of 8 memory chips), its borrow input goes high. This is the data input to the clock latch and sets the latch on the next system clock pulse.

The output of the clock latch also drives the DATA AVAIL L signal back to the Display Processor to indicate that the data it was seeking is now available on the Data Bus. Two pair of drivers are enabled, one with the Interlace ROM control signal OUT LO BYTE H, and the other with OUT HI BYTE H. These drivers send B RAM Data 0--3 back down the Data Bus to the Display Processor.

The cycle ends when the Display Processor withdraws the WRITE signal and the D REQ DATA L signal.

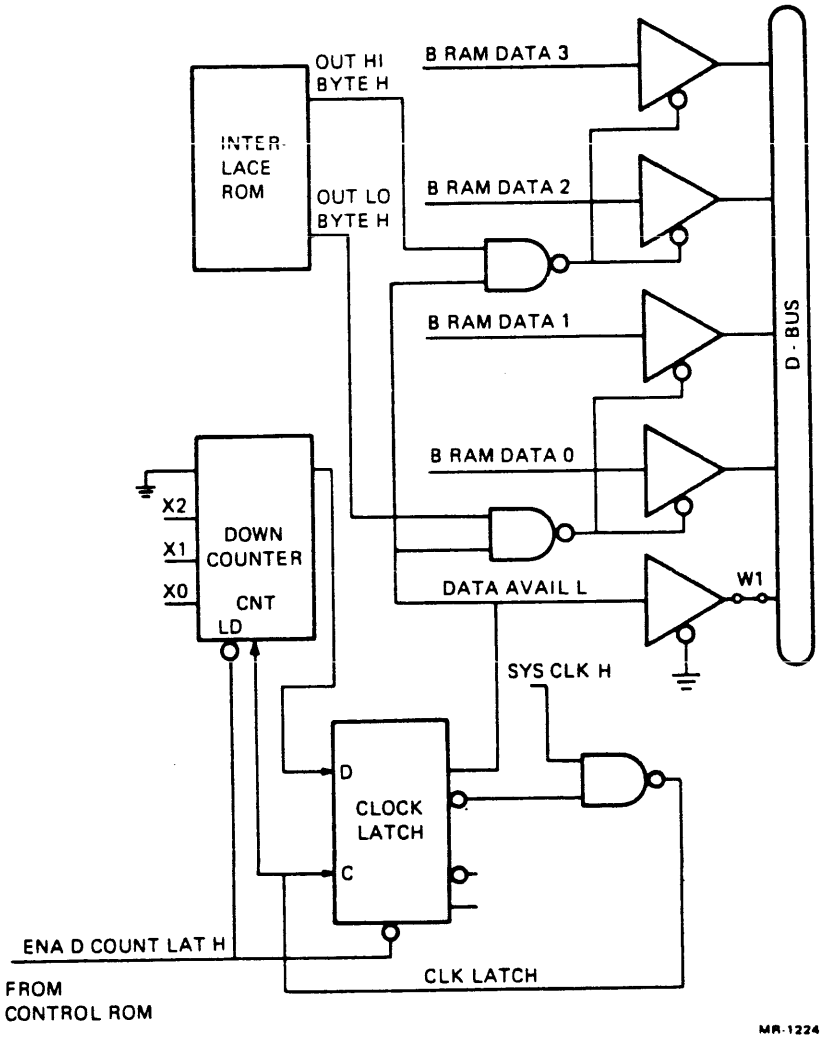


Figure 5-18
Pixel Read-Back Logic

CHAPTER 6

M7061 SYNC GENERATOR/CURSOR CONTROL TECHNICAL DESCRIPTION

6.1 INTRODUCTION

The M7061 Sync Generator/Cursor Control module synchronizes VSV11/VS11 system operations, provides digital-to-analog conversion (DAC) for data displayed on the system monitor, and contains cursor control circuits for the generation and placement of crosshairs (cursor) on the system monitor. The cursor control circuits operate with the H3060 Joystick, supplied with VSV11/VS11 systems.

6.2 GENERAL DESCRIPTION

A block diagram of the M7061 is shown in Figure 6-1. The Sync Generator circuits produce EIA RS-170 standard waveforms which may be selected to a 50 Hz or a 60 Hz frame rate and to Interlaced or Non-Interlaced scans. The blanking and sync signals from the Sync Generator circuits are applied to the backplane Video Bus to synchronize the display system. These signals are enabled to the backplane on only one M7061 per VSV11/VS11 subsystem.

The DAC and Sync Stripper circuits perform in two modes: stand alone mode and slave mode. During stand alone operation (sync is generated internal to the M7061), four bits of data are received from the Image Memory via the Video Bus along with a composite sync (COMP SYNC) signal. The data and composite sync are applied to a DAC where they are combined and converted into a composite video signal. The composite video signal can be applied to a black and white composite video CRT monitor (COMPOSITE VIDEO OUT). Since the DAC is a four bit DAC, 16 intensity levels (levels of gray) can be displayed. Alternately, the output of the DAC can drive a Red-Green-Blue (RGB) color CRT monitor where the Green output (COMPOSITE VIDEO OUT) supplies the sync for the color monitor. Data input to the DAC is gated by the Blink logic to allow for "blinking" (flashing off and on) of selected pixels on the screen.

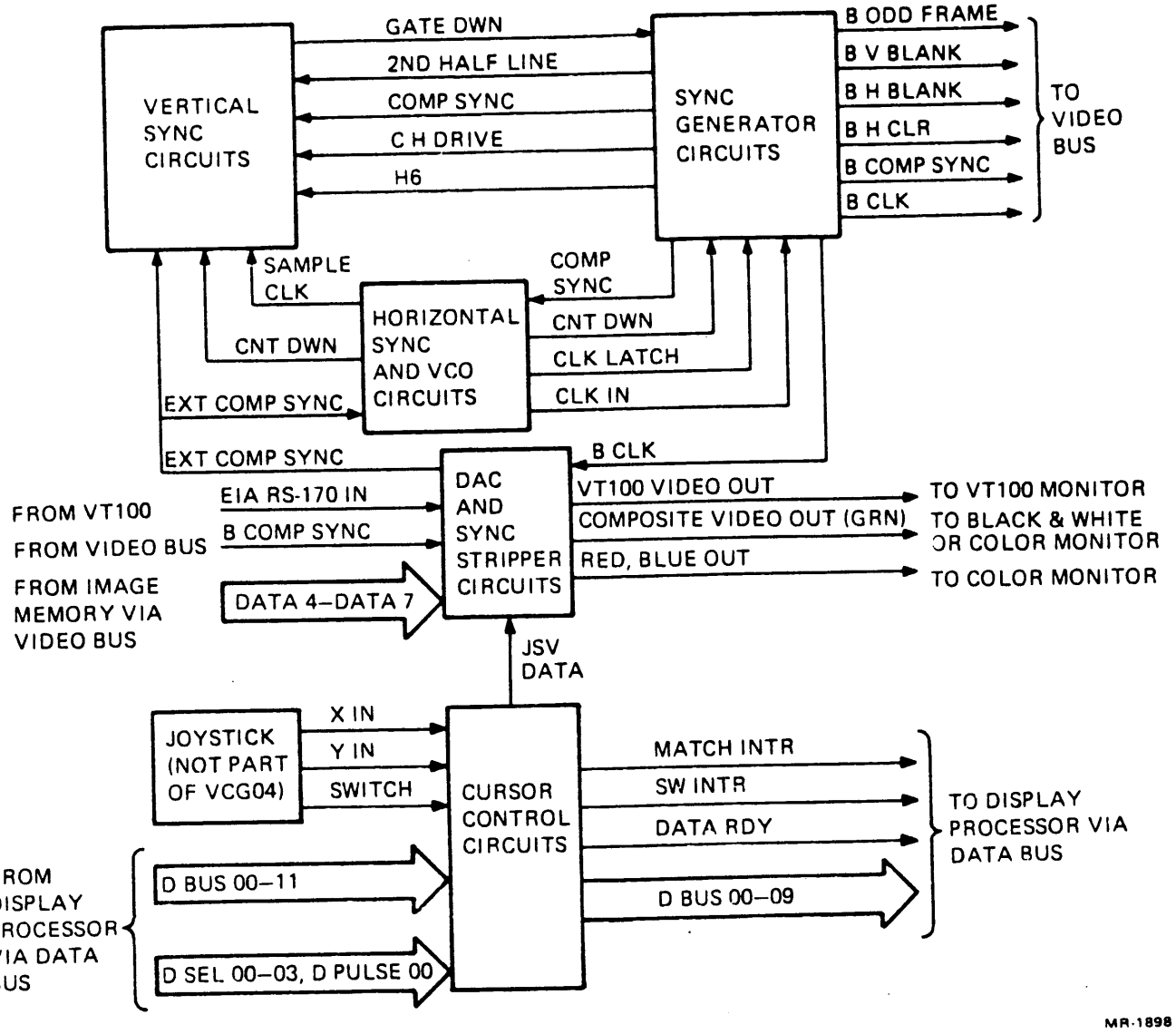


Figure 6-1
M7061 Basic Block Diagram

During slave operation (the M7061 is receiving sync and video information from another source, such as a VT100), a composite video RS-170 signal is received by the DAC and Sync Stripper circuits. The Sync Stripper removes the sync pulses from the composite video signal and applies them, as external composite sync (EXT COMP SYNC), to the Horizontal and Vertical Sync circuits to lock the horizontal and vertical scans. Meanwhile, the video portion of the composite video signal is applied to a video mixer where video data from the Video Bus can be added to the video on the incoming RS-170 signal. This mixing action produces a new composite video signal which can be applied to a composite video monitor. The composite video monitor is normally a VT100. The composite video signal is also applied to the Green input of a composite video color monitor, such as the VRV02.

The Horizontal Sync and VCO circuits operate in two modes: internal and external. In the internal mode a 25.1748 MHz crystal oscillator supplies the clock signal which is divided by 20 to produce SAMPLE, CLK, CLK LATCH, and CNT DWN (count down). These are used for timing reference throughout the Sync Generator. In external mode, the EXT COMP SYNC signal is composed of sync pulses which the Sync Stripper removed from the incoming RS-170 composite video signal from an external source. These are phase compared to the internally generated COMP SYNC signal from the Sync Generator circuits. The output of the Phase Detector drives a voltage controlled oscillator (VCO). If the two COMP SYNC signals are in phase the output frequency of the VCO remains constant. If the signals are not in phase, the VCO frequency changes the clock rate to the Sync Generator circuits and thus changes the internal COMP SYNC rate. When the EXT COMP SYNC and the internal COMP SYNC signals are in phase, the Sync Generator is phased-locked to the external source.

The Vertical Sync circuits synchronize vertical counters to the incoming RS-170 EXT COMP SYNC when operating in the external (VT100) mode. This is accomplished by comparing the EXT COMP SYNC and the 2ND HALF LINE signal from the Sync Generator, and the internal COMP SYNC and samples generated within the Vertical Sync circuits. If the signals do not match, GATE DWN causes the Vertical Counters to count down until a match occurs. When a match does occur, the Vertical Counters are sync-locked to the external source.

The Cursor Control circuits produce the crosshairs (cursor) for display on the system monitor, and generate the Joystick Switch and Cursor Match interrupts when enabled with the Joystick Status instruction (Chapter 3). When the Joystick is connected, joystick positioning voltages (X IN and Y IN) are applied to the Cursor Control circuits. The analog X IN and Y IN control the X and Y cursor positions by counting the position values up or down depending on the polarity and magnitude of the input voltages. The X and Y positions are processed and applied as joystick video data (JSV DATA) to the DAC circuits for display on the system monitor as crosshairs representing the joystick position. It should be noted that the joystick used with the Sync Generator is

a rate-type joystick. That is, small movements of the joystick produce small movements of the crosshairs. Large joystick movements cause the crosshairs to move rapidly on the system monitor. The X and Y joystick position registers can also be written by the Display Processor, allowing software programs to move the cursor.

Two types of Display Processor interrupts can be generated from the joystick via the Cursor Control circuits. The first is the Joystick Switch interrupt and the second is the Cursor Match interrupt. The Joystick Switch interrupt occurs whenever the joystick pushbutton is pressed, provided the Switch Interrupt and Switch Interrupt Enable bits were issued by the Joystick Status instruction. The Match Interrupt occurs when the cursor position "matches" an Image Memory pixel location which is being written by the Display Processor. The Image Memory pixel location is supplied by the Display Processor (D BUS <11:00>) and compared to the joystick position. Joystick Status instruction Match Interrupt Enable and Match Interrupt bits must be set to enable the Cursor Match interrupt. When either the Switch interrupt or the Match interrupt is generated, the X- and Y- position of the joystick is transfered to the DXR and DYR status registers of the Display Processor. The effect of the external joystick switch being pressed can also be simulated by the Display Processor, which can set a bit in the Cursor Control curcuit; this bit is ORed with the external Switch input so that either signal can cause an interrupt.

6.3 FUNCTIONAL DESCRIPTION

The paragraphs which follow contain a functional description of the major Sync Generator/Cursor Control functions. Each function introduced in Figure 6-1 is expanded and supported with a detailed block diagram. Additionally, the +5 Vdc to -5 Vdc Converter and the Video Bus are discussed. These are not shown in Figure 6-1. As a prelude, a discussion on raster scanning techniques is provided.

6.3.1 Scanning Techniques

In addition to providing synchronizing signals to the Image Memory and the Display Processor modules, the Sync Generator supplies a composite video signal to a composite video CRT monitor. The composite video signal contains vertical and horizontal sync pulses to control the vertical and horizontal scans of the CRT monitor. The M7061 is used with composite video CRT monitors with either Non-Interlaced or Interlaced scans.

6.3.1.1 Non-Interlaced Scanning -

In a Non-Interlaced scan, the picture is traced on the CRT with one excursion of the CRT electron beam starting at the top of the screen and ending at the bottom. This one excursion from top to bottom is also referred to as a field or a frame. When the Sync Generator is operating in the Non-Interlaced mode, 262 horizontal scan lines are produced for 60 Hz operation and 315 are produced for 50 Hz. Only 240 (60 Hz) and 256 (50 Hz) of these scan lines are visible on the screen. The lines not seen are blanked out during vertical retrace time while the beam is moving from the bottom to the top of the screen.

Figure 6-2 illustrates the scanning for a Non-Interlaced CRT monitor along with synchronizing and blanking as determined by the Sync Generator. The first scan line (raster line) starts at the upper left of the CRT screen and sweeps towards the right. At the right, horizontal sync causes the CRT electron beam to do a horizontal retrace. Horizontal retrace is the rapid movement of the beam from the right to the left side of the screen. Horizontal retrace occurs during horizontal blanking time.

Horizontal blanking is a signal which indicates to the graphic system video circuits that video should stop since horizontal retrace is approaching. Horizontal sync causes the CRT monitor to retrace for the start of the next line. As shown in Figure 6-3, horizontal blanking preceeds horizontal sync and causes raster blanking at the right of the screen. This is done to ensure that all video has stopped before the retrace. When the electron beam reaches the left of the screen, horizontal blanking is removed and allows video to the CRT monitor. This beam sweeping, synchronization, and blanking process continues until the last raster line. When the last raster line (at bottom of CRT) reaches the right side of the screen, Horizontal Sync and Vertical Sync pulses cause the electron beam to move back to the upper left of the CRT screen. During the beam's travel upward, the beam is swept towards the left and then to the right in a zigzag fashion to reach the top of the CRT. This zigzag motion is caused by the horizontal syncs occurring during the upward retrace of the beam. Horizontal retrace continues during the vertical retrace time. When the electron beam reaches the upper left, vertical blanking ends and the beam again starts tracing horizontal lines from top to bottom. The relationship between vertical blanking, horizontal blanking, and horizontal sync for the Sync Generator is shown in Figure 6-4.

6.3.1.2 Interlaced Scanning -

During an Interlaced scan (Figure 6-5), the picture is traced on the CRT with two successive excursions of the CRT electron beam. Each excursion is referred to as a field. Thus, there are two fields and the two fields equal one frame. The fields are called even and odd and have the same number of scan lines.

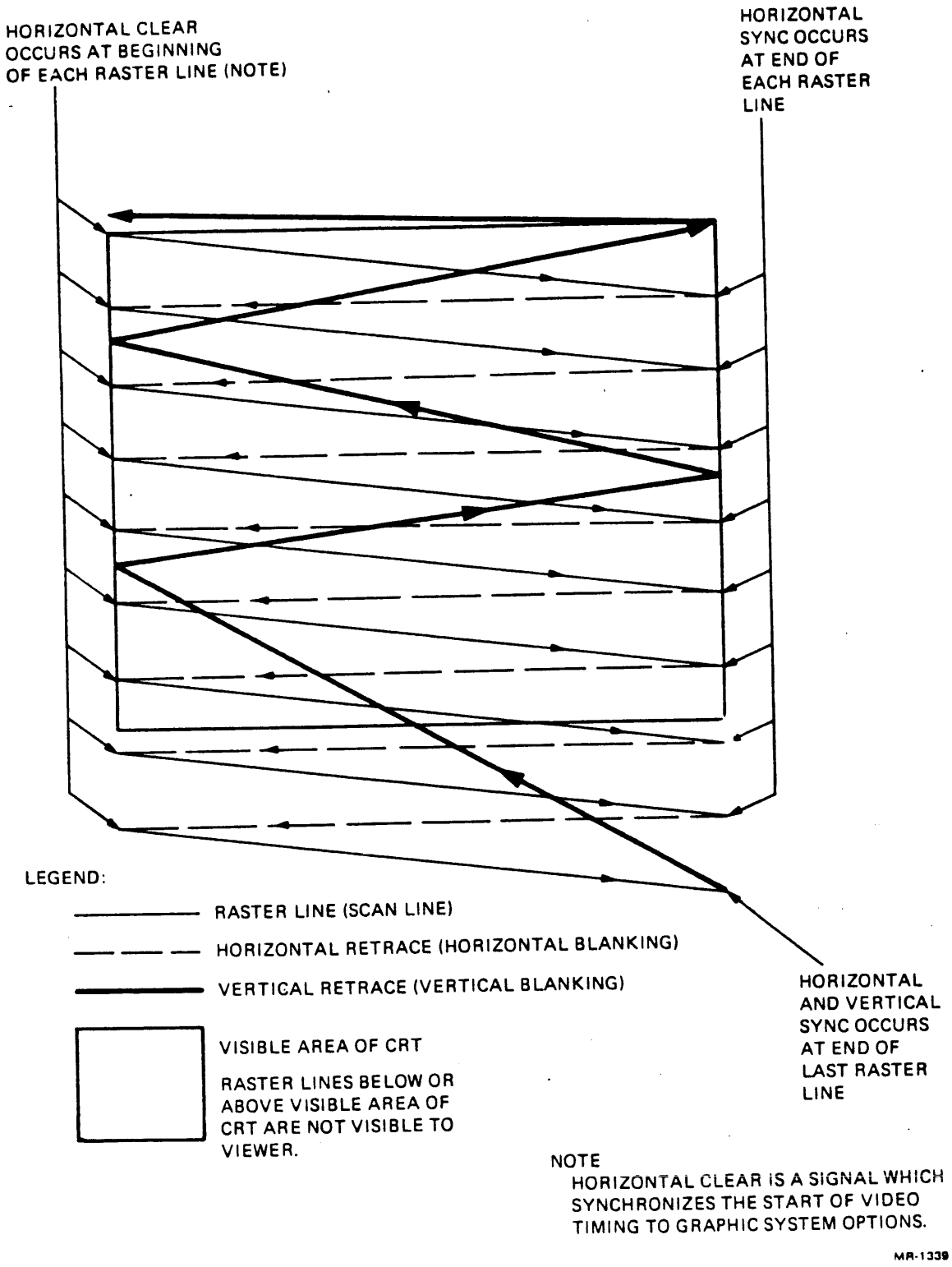


Figure 6-2
Non-Interlaced Scanning

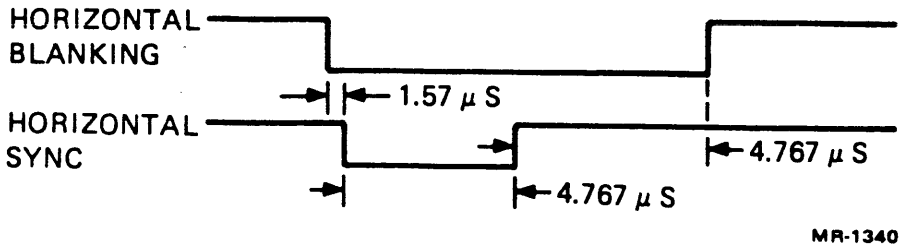


Figure 6-3
M7061 Horizontal Blanking and Sync Times

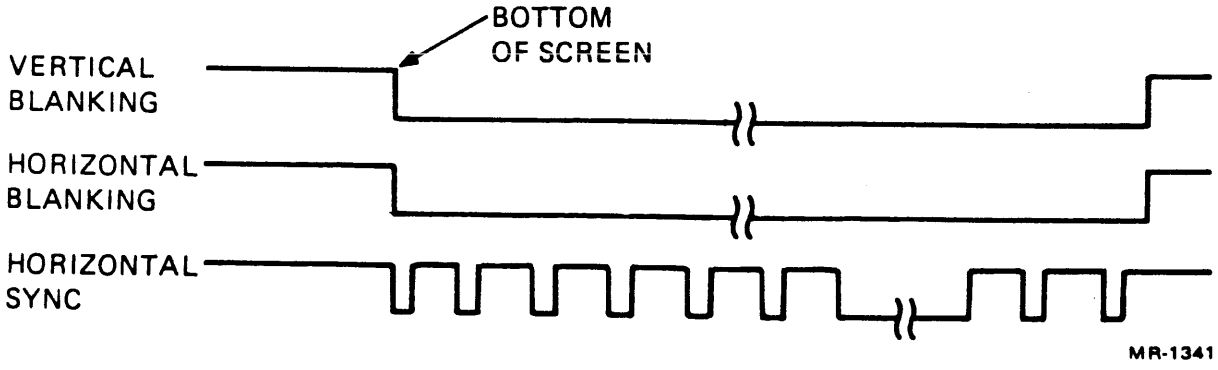


Figure 6-4
M7061 Vertical Blanking, Horizontal Blanking,
and Sync Relationship

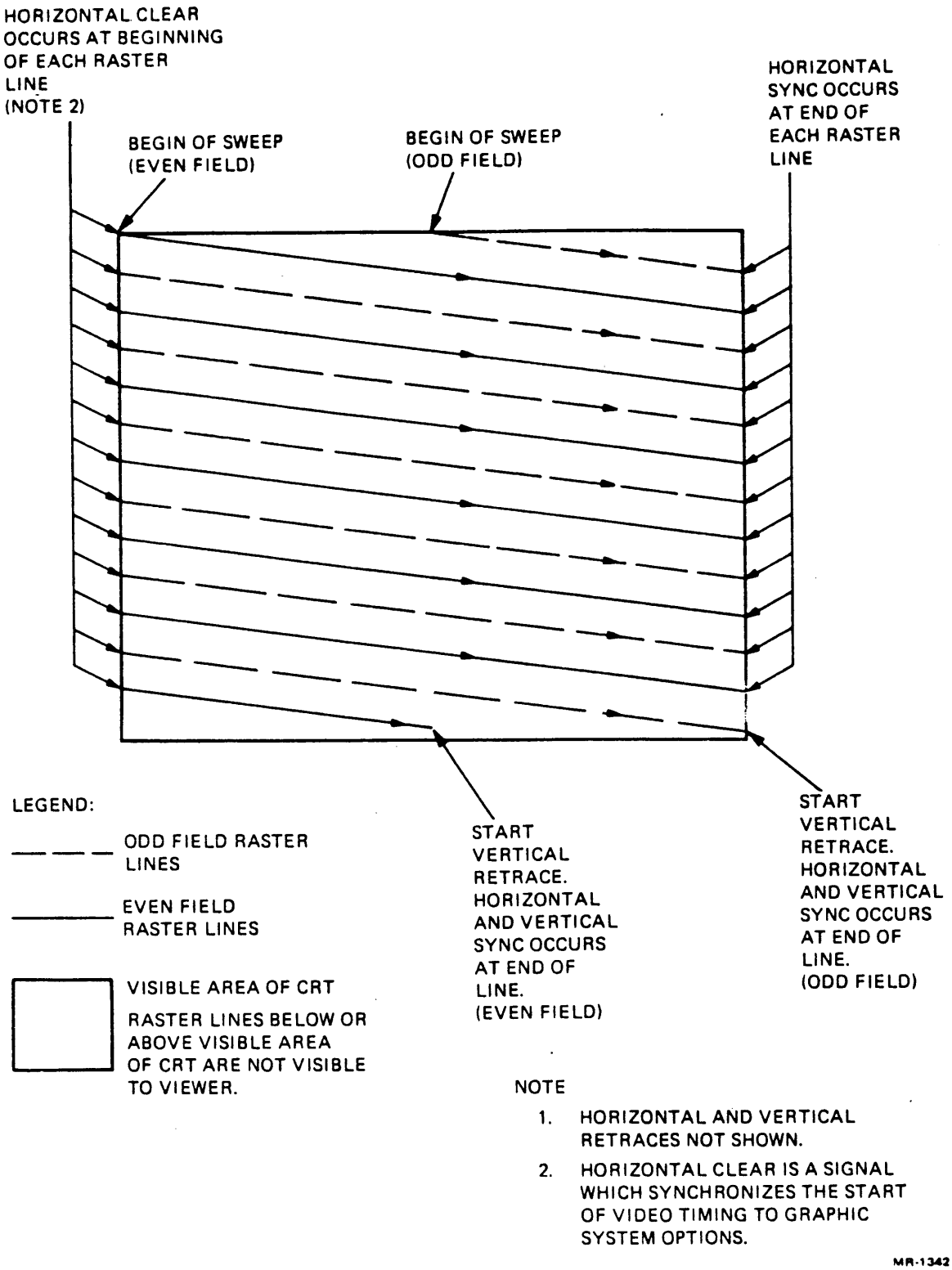


Figure 6-5
Interlaced Scanning

When the Sync Generator is operating in the Interlaced mode, 525 horizontal scan lines (both fields) are produced for 60 Hz operation and 629 (both fields) are produced for 50 Hz. Of these scan lines 480 (60 Hz) and 512 (50 Hz) are visible on the screen. The lines not seen are blanked out during vertical retrace time while the beam is moving from the bottom to the top of the screen.

Figure 6-5 illustrates the scanning for an Interlaced CRT monitor along with synchronizing and blanking as determined by the Sync Generator. The odd field starts at the top center of the CRT and traces approximately one-half length of a raster line. When the CRT beam reaches the right side of the screen, horizontal blanking occurs. Horizontal sync (Figure 6-3) causes the beam to sweep to the left of the CRT during horizontal retrace. This process continues until the beam reaches the lower right corner of the CRT. At the lower right, horizontal sync and vertical sync pulses cause the electron beam to move back to the top of the CRT screen in a zigzag fashion, as described for Non-Interlaced scanning. To avoid confusion, vertical and horizontal retraces are not shown in Figure 6-5.

The even field raster lines are traced from top to bottom like the odd field lines. However, the even field lines start in the upper corner of the CRT and are traced in-between the odd field raster lines. Vertical retrace for the even field occurs at the end of the last raster line which is approximately at the bottom center of the screen.

For 60 Hz operation, 262.5 raster lines are traced on the screen for each field. This gives a raster line total of 525 lines per frame. During 50 Hz operation 314.5 raster lines are traced per field for a total of 629 lines per frame.

6.3.2 Sync Generator Circuits

The Sync Generator circuits produce EIA RS-170 waveforms for vertical blanking, horizontal blanking, and composite sync for use throughout the graphic system. These waveforms, along with clear and clocking pulses, are generated by Vertical and Horizontal counters which address Vertical and Horizontal ROMs within the Sync Generator. The RS-170 waveforms from the Sync Generator circuits are applied to the system Video Bus for distribution.

Figure 6-6 shows a detailed block diagram of the Sync Generator circuits. A clock signal (CNT DWN) from the Horizontal Sync-Up and VCO circuits clocks the horizontal counters until the counters overflow. The overflow generates a carry (CRY) from the horizontal counters which starts the vertical counters. Outputs H1 through H6 from the horizontal counter address the Horizontal ROM. The H1 through H6 inputs to the ROM enable the ROM to produce the horizontal clear, blanking, and composite sync

signals which are required by the graphic system during a horizontal line time. These horizontal signals are fed to a latch. When the latch is clocked (CLK LATCH C) by the horizontal sync and VCO circuits, the horizontal signals are passed to the 3-state drivers. The drivers are enabled and place the signals onto the video bus.

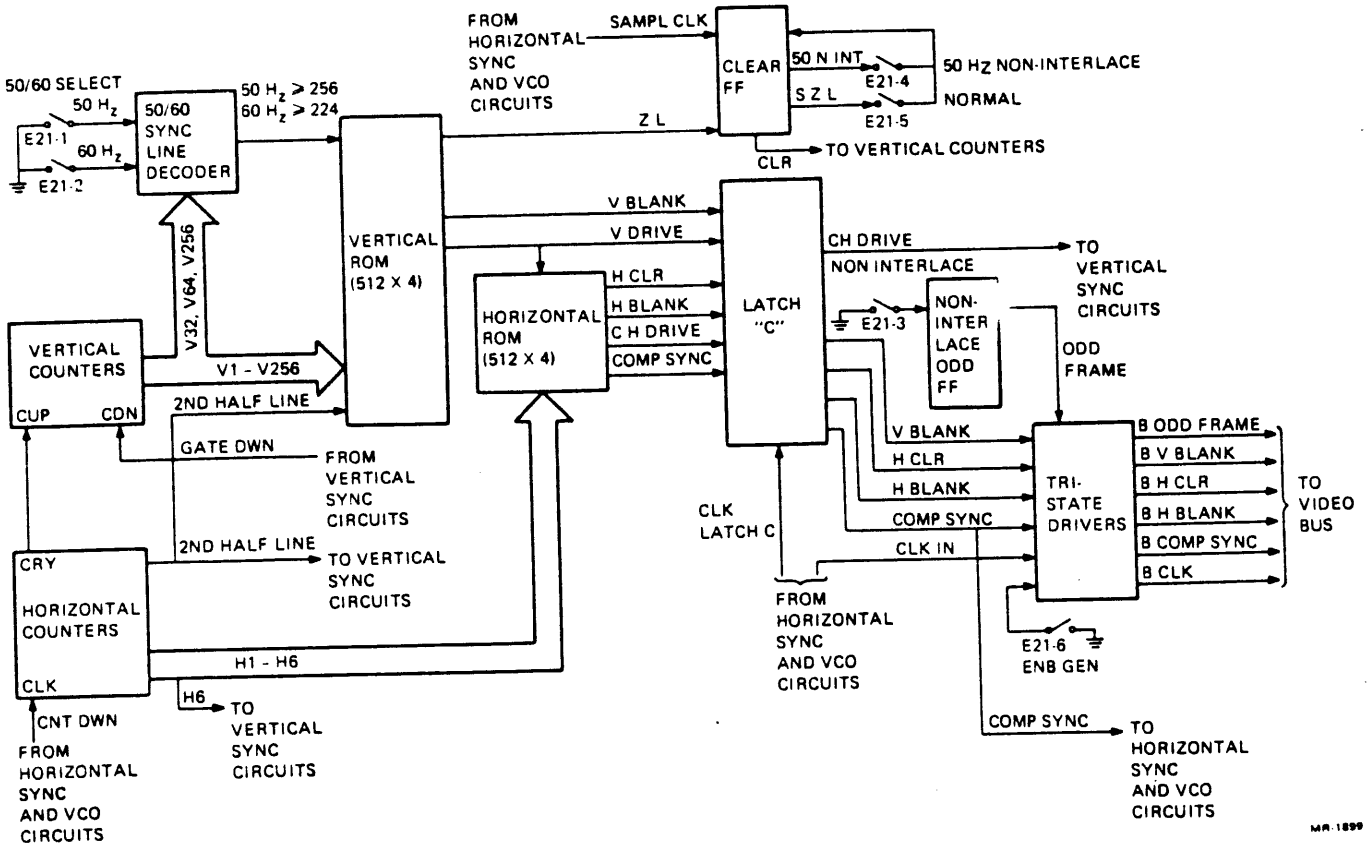


Figure 6-6
M7061 Sync Generator Circuits -- Detailed Block Diagram

H BLANK includes a front porch, horizontal sync, and a back porch. C H DRIVE is used during vertical blanking for sync sampling.

COMP SYNC is a pulse which occurs in the middle of H BLANK. COMP SYNC is comprised of the horizontal sync pulse intervals, the equalizing pulse intervals, and the vertical sync pulse intervals. The Horizontal Counter's 2ND HALF LINE output is applied to the Vertical ROM during the vertical retrace to control external sync.

When the Horizontal Counters overflow, the Vertical Counters are incremented. The rate of the count-up (or the line time) is determined by the carry from the Horizontal Counters. In the internal sync generation (standalone) mode, an internal 25.1748 MHz crystal oscillator in the Horizontal Sync and VCO circuits supplies the clock to the Horizontal Counters. During External Sync (slave) mode ("VT100 mode"), the clock is supplied by a VCO in the Horizontal Sync and VCO circuits. The VCO phase locks to the composite sync (EXT COMP SYNC) supplied by an external source (VT100). Regardless of the clock source, the Vertical Counters count the number of lines on the CRT monitor screen. Vertical Counter (V1-V256) outputs address the Vertical ROM and apply V32, V64, V256 to the 50/60 Sync Line Decoder. The Vertical ROM produces vertical blanking and drive signals which are latched by the LATCH CLK signal. V BLANK is placed on the Video Bus via the 3-state drivers.

The 50/60 Sync Line Decoder allows the Sync Generator to operate with either 50 Hz or 60 Hz power sources, thus eliminating display jitter caused by 10Hz nonsynchronous operation. 50 Hz or 60 Hz selection is by means of two switches (E21-1, E21-2) on the Sync Generator module. These switches determine when the output of the 50/60 Sync Line Decoder goes high and changes one of the address inputs to the Vertical ROM. The 50/60 Sync Line Decoder is enabled when the Vertical Counters reach a line count of 128. If the 50 Hz switch (E21-1) is closed and V32 and V64 from the Vertical Counters are high, 50/60 Sync Line Decoder output 50 Hz $\geq$ 256 goes high. On the other hand, if the 60 Hz switch (E21-2) is closed (50 Hz switch open), the decoder output 60 Hz $\geq$ 224 goes high when the Vertical Counters reach line 224 or greater.

When the 50 Hz $\geq$ 256/60 Hz $\geq$ 224 output to the Vertical ROM goes high 16 additional lines are counted for 50 Hz and 32 additional for 60 Hz. The graphic system then goes into vertical blanking time. The 50/60 Sync Line Decoder saves ROM space for redundant counts and allows the count to continue until the appropriate number of lines has been reached. The V DRIVE output is applied to the latch and indicates the system has entered the vertical retrace interval. V DRIVE is also applied as an address input to the Horizontal ROM which causes serrations (equalizing pulses) to be supplied along with the vertical blanking as part of the COMP SYNC signal. That is, during the first part of the V BLANK interval, the Sync Generator produces an equalizing pulse interval, a vertical interval, and another equalizing pulse

interval.

As mentioned previously, the Sync Generator can be selected to provide sync and blanking for Interlaced and Non-Interlaced scans, and can also be selected for compatible operation with the VT100 monitor. When the Non-Interlace mode is selected on the Sync Generator, the Non-Interlace Odd flip-flop is held in the reset state. This causes the Sync Generator to produce only even fields on the system monitor. The output of the Non-Interlace Odd flip-flop is applied to the 3-state driver which places the ODD FRAME signal on the Video Bus.

When the ODD FRAME line is low (Non-Interlace switch open) the system performs an odd field scan. Even field scans are performed when the ODD FRAME line is high (Non-Interlace switch closed). With the switch open the Non-Interlace Odd flip-flop is allowed to toggle upon the completion of each field.

The 50 Hz Non-Interlace and Normal switches determine the mode of operation; i.e., 314-line normal RS-170 50 Hz Non-Interlace or 315-line VT100 50 Hz Non-Interlace. During normal mode, SAMPLE CLK is gated with Z L. This produces SZ L which is applied as a clock to a Clear flip-flop which clears the vertical counters. This clear generates a clear to the vertical counters after a line count of 314. For VT100 mode operation, SAMPLE CLK is gated with Z L but this time 50 N INT is produced. 50 N INT is applied to the Clear flip-flop. The Clear flip-flop now clears the vertical counters after a line count of 315.

The Z L output signal from the ROM occurs twice in succession in the ROM code. The 50 N INT signal provides a count of two before actually clearing the vertical counters.

Only one Sync Generator circuit is required in a graphic system. The Sync Generator has one four-bit digital-to-analog converter (DAC) and can handle only four bits of video data. A VSV11/VS11 graphic system may use up to four Sync Generator modules. Only one of these modules would be controlling the synchronization; this module is termed the "Master". The other three, termed "Slaves", would have the Sync Generator circuits disabled because the Master module provides all the signals required for synchronization. The Sync Generator circuits are disabled by opening switch E21-6 and jumper W19 on the designated Slave modules. This disables the 3-state drivers to the Video Bus.

6.3.3 DAC And SYNC Stripper Circuits

The DAC and Sync Stripper circuits perform four functions:

1. Convert four-bit video data from the Image Memory to analog intensity data.

2. Disable (blink) pixel data.

3. Convert joystick video data from the cursor control circuits to analog intensity data for the system monitor crosshairs (cursor).

4. Separate the sync pulses from the video information during operation in External Sync mode, where an EIA RS-170 signal is applied to the DAC and Sync Stripper circuits.

A detailed block diagram of the Sync Generator DAC and Sync Stripper circuits is shown in Figure 6-7.

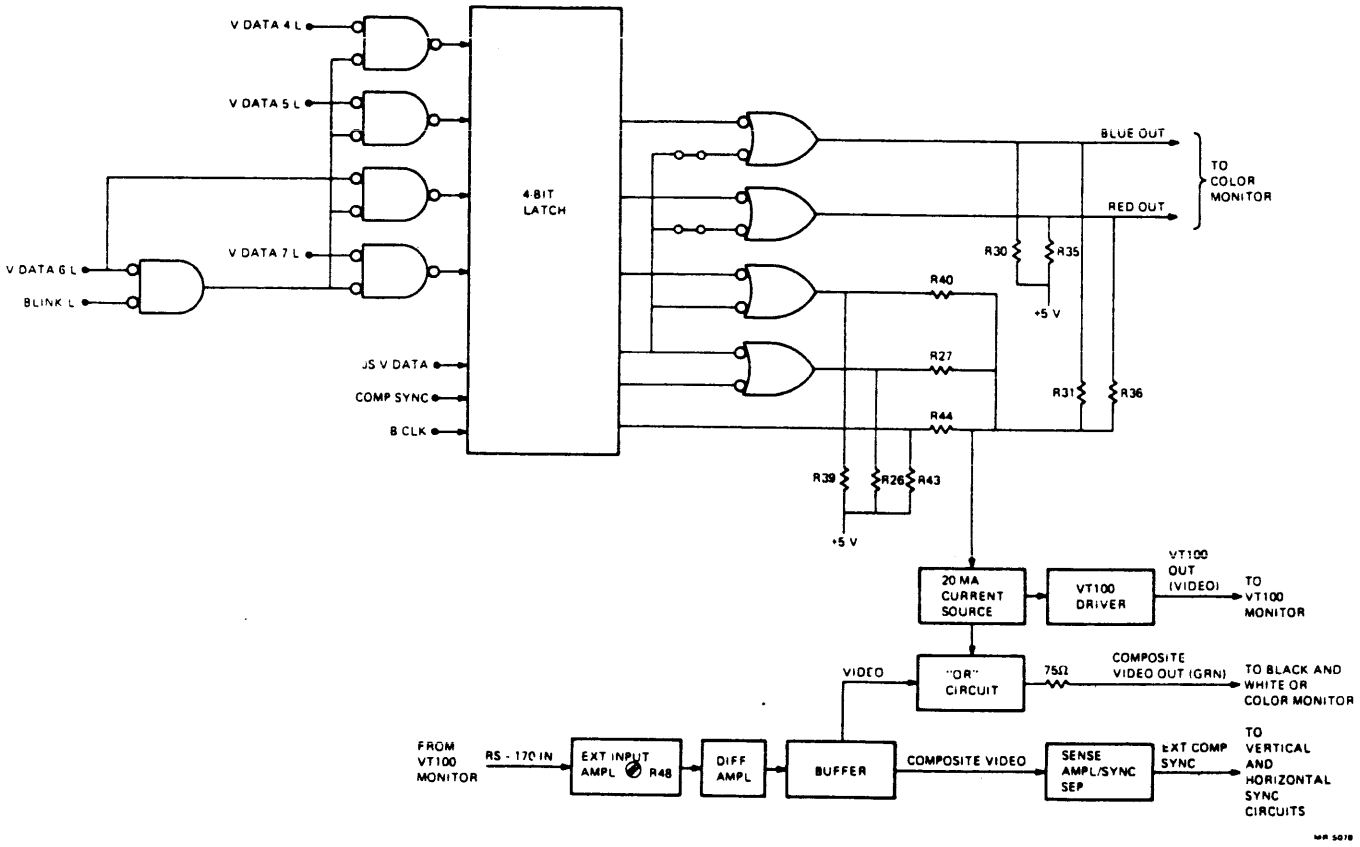


Figure 6-7
M7061 DAC and Sync Stripper Circuits --
Detailed Block Diagram

6.3.3.1 DAC Circuits -

The DAC (Digital-to-Analog Converter) circuits in Figure 6-7 include the four-bit latch and the 20 mA current source. Four bits of video data from the Image Memory are received by the Blink circuits (gates). The video data is blocked fifty percent of the time if the Blink circuits are enabled and video data bit 6 is true for that pixel. The video data is then received by the four-bit latch from the video bus. When B CLK goes high, the data bits (DATA 04--DATA 07) are latched. The output of the four-bit latch feeds (through resistors) a 20 mA current source. The four-bit latch, the resistors, and the 20 mA current source form a current source type DAC. When one or more of the four data bits is low (off), current is removed from the 20 mA current source. If all four bits are low, all the current (except for a small bias current of 0.7 mA) is taken away from the 20 mA current source. Changing the state of the data input bits changes the level of current supplied by the 20 mA current source and thus changes the voltage level applied to the VT100 driver and the "OR" circuit. In addition to the four data bits, the B COMP SYNC (from with the active Sync Generator circuits) is applied to the four-bit latch via the Video Bus. B COMP SYNC also removes current from the 20 mA current source, thereby adding synchronizing pulses (horizontal syncs and serrations) to the video data from the Video Bus. This results in a composite video signal at the output of the 20 mA current source. The composite video signal is applied to the VT100 monitor via the VT100 driver and/or to a black and white monitor (or the Green gun of a color monitor) via the "OR" circuit.

Input bits 06 and 07 of the 4-bit latch are both driven by JSV DATA from the Cursor Control circuits for the display of the system monitor crosshairs. Bits 04 and 05 can be driven if selected by the jumpers. JSV DATA is pulsed for the display of the vertical crosshair, and is held low (intensity on) for either 17 pixels of one horizontal line or for the entire horizontal line, for display of the horizontal crosshair. The size of the crosshair is determined by jumper W17.

For black and white operation, the four-bit DAC provides for 16 levels of grey (including black). For color operation, two outputs from the four-bit latch feed open collector drivers. These drivers can be used to supply red and blue video information to a color monitor. The remaining two bits of Green video information pass through the 20 mA current source and the "OR" circuit to drive the Green gun in the color monitor. The Green output provides four levels of green along with synchronizing signals. The range of output voltage at the green output is 0 V through 1.6 V into a 75 ohm impedance.

6.3.3.2 Sync Stripper Circuits -

The Sync Stripper circuits in Figure 6-7 include the External Input Amplifier, the Differential Amplifier, the Emitter Follower, the Buffer, and the Sense Amplifier/Sync Separator. These circuits remove the sync pulses from an EIA RS-170 composite video signal which is supplied by the VT100 monitor. An EIA RS-170 waveform in the range of 0 V to 1.4 V is applied to the External Input Amplifier. The gain of this amplifier is adjustable by means of potentiometer R48. From the External Input Amplifier, the level-adjusted RS-170 signal is applied to the Differential Amplifier. The Differential Amplifier has a dc gain of 2, an ac gain of 7.5, and a cut-off frequency of 15 Hz. The output from the Differential Amplifier is applied to an emitter follower. At the Emitter Follower, the most negative signal excursions (sync tips) are clamped to -0.6 V. The -0.6 V sync tips are applied to the Buffer. The signal level at the output of the Buffer ranges from 0 V to +2.8 V, with the lower +0.8 V being the sync signal. The output of the buffer is applied to the Sense Amplifier/Sync Separator. The Sense Amplifier/Sync Separator is biased off at +0.4 V. This results in a low output from the Sense Amplifier/Sync Separator for inputs below 0.4 V, and a high output for inputs greater than 0.4 V. Thus, the output (EXT COMP SYNC) from the Sense Amplifier/Sync Separator consists of only the synchronization signal which includes all of the serrations and equalizing pulses. This sync signal is then applied to the Vertical and Horizontal Sync circuits where it is used to synchronize the Vertical and Horizontal Counters.

In addition to the sync output from the Sync Stripper circuit's buffer, the buffer provides EIA RS-170 video to the "OR" circuit. The "OR" circuit mixes the incoming (from the VT100 monitor) video with the composite video from the 20 mA current source. This results in a composite video signal containing video data and sync from the Video Bus, and video data from the EIA RS-170 input from the VT100 monitor. The output voltage level can be adjusted by R9.

6.3.4 Horizontal Sync And VCO Circuits (Phase Lock Loop)

The Horizontal Sync and VCO circuits produce clock signals for the Sync Generator logic. These clock signals can be derived from an internal crystal oscillator (INTERNAL CLK) or from a voltage controlled oscillator (VCO) which changes frequency as the result of comparing the EXT COMP SYNC signal from the DAC and Sync Stripper circuits to the COMP SYNC signal from the Sync Generator circuits. A detailed block diagram of the Horizontal Sync and Clock circuits is shown in Figure 6-8.

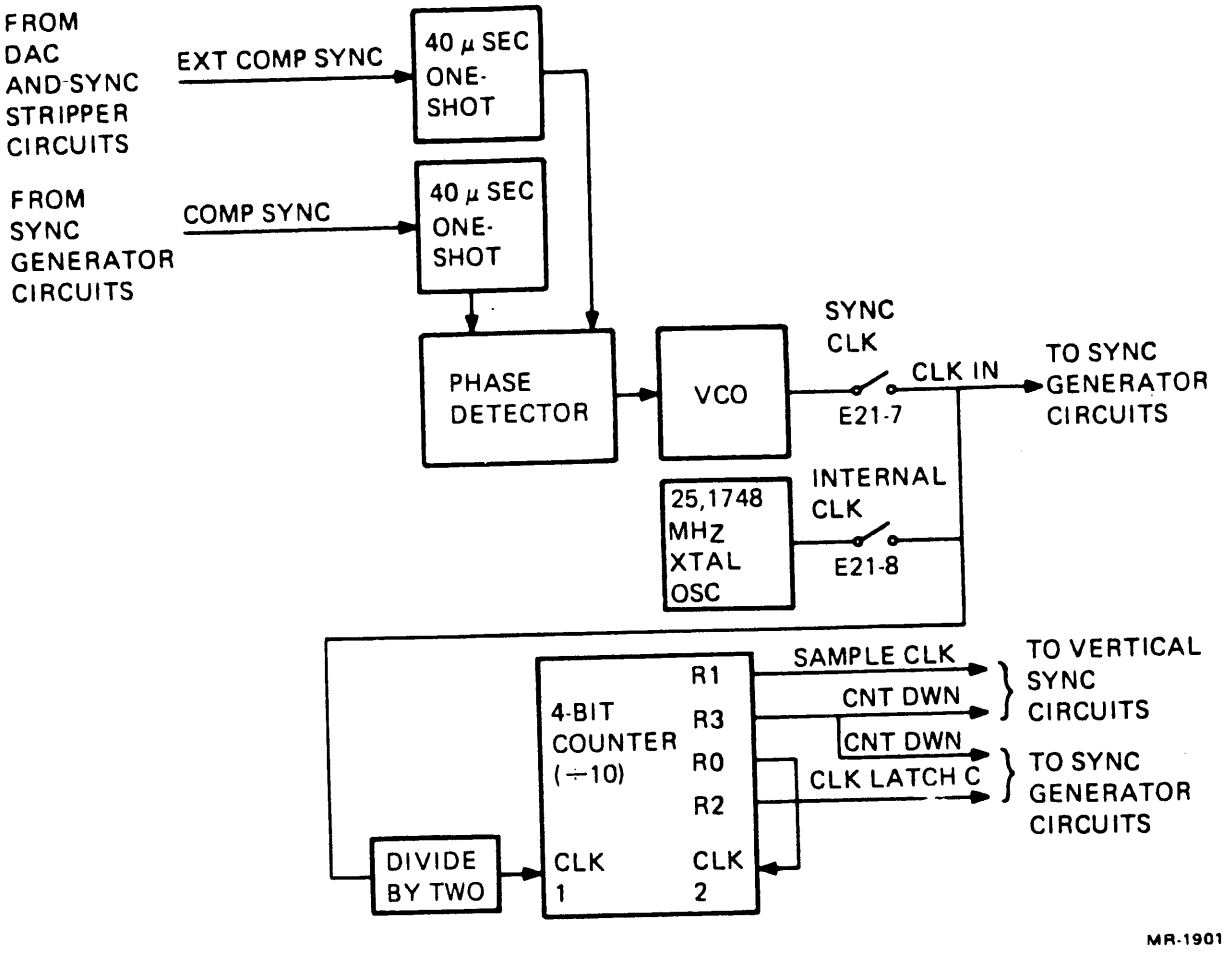


Figure 6-8
M7061 Horizontal Sync-Up and VCO Circuits --
Detailed Block Diagram

When operating in Internal Sync mode (INTERNAL CLK switch E21-8 closed, SYNC-UP CLK switch E21-7 open), the output from the 25.1748 MHz crystal oscillator is divided by 2 and clocks the four-bit counter. This counter divides the input by 10 and produces clock signals for the Vertical Sync and Sync Generator circuits.

When operating in External Sync mode (VT100 mode) (INTERNAL CLK switch E21-8 open, SYNC-UP CLK switch E21-7 closed), the phase relationship between the EXT COMP SYNC signal (from the DAC and Sync Stripper circuits) is compared to the COMP SYNC from the Sync Generator circuits. If the two signals are out of phase, the control voltage to the VCO changes, changing the output frequency (CLK IN) from the VCO. This changes the clock to the four-bit counter, and thus changes the clock rates which drive to

the Vertical Sync Sync Generator circuits. Since the clock to the Sync Generator has changed, the rate (and thus the phase) of COMP SYNC from the Sync Generator changes. These changes will continue until the phase relationship between EXT COMP SYNC and COMP SYNC match. When the phase matches, the voltage to the VCO stabilizes and the VCO output frequency (CLK IN) stabilizes. Under this condition, the Sync Generator circuits are phase-locked to the horizontal sync from the VT100.

The 40 uS (microsecond) one-shots prevent the Phase Detector from locking-up on half-line data and causing clocking errors. Half-line data includes the vertical retrace interval and equalizing pulses which are part of the COMP SYNC signal. Since the Phase Detector operates on a high to low transition, the Phase Detector would try to sync to the equalizing pulses. This would cause the VCO to shift up and down in frequency, hunting for a phase match between the everchanging pulses and the EXT COMP SYNC signal.

6.3.5 Vertical Sync Circuits

The Vertical Sync circuits synchronize the vertical counters in the Sync Generator circuits to the incoming EIA RS-170 signal from the VT100 monitor when operating in the External (VT100) mode. A detailed diagram of the Vertical Sync circuits is shown in Figure 6-9.

Vertical Sync is accomplished by using the EXT COMP SYNC signal as a reference, and producing a sample window during the vertical retrace interval. The sample window is provided by horizntal timing which is synchronized to the incoming horizntal sync pulses by the Horizontal Sync and VCO circuits. During the sample window, if the COMP SYNC signal does not match the EXT COMP SYNC signal the M7061 vertical counters are gated down until a match occurs. Three samples per field are made during the vertical retrace interval.

When the horizontal counters are synchronized, the Vertical Sync circuits receive synchronized horizontal clock signals. The EXT COMP SYNC and 2ND HALF LINE signals are NANDed in the Vertical Sync circuits. When 2ND HALF LINE goes low (at the left half of a line), the gate is enabled and a high "D" input is provided to the Pre-Sample flip-flop. This occurs during horizontal sync or the vertical retrace interval. The Sync Generator produces H6 (H6 happens at quarter line time) to clock the Pre-Sample flip-flop. The setting of the Pre-Sample flip-flop during H6 time starts the sample window, and indicates the EXT COMP SYNC is at the vertical retrace interval.

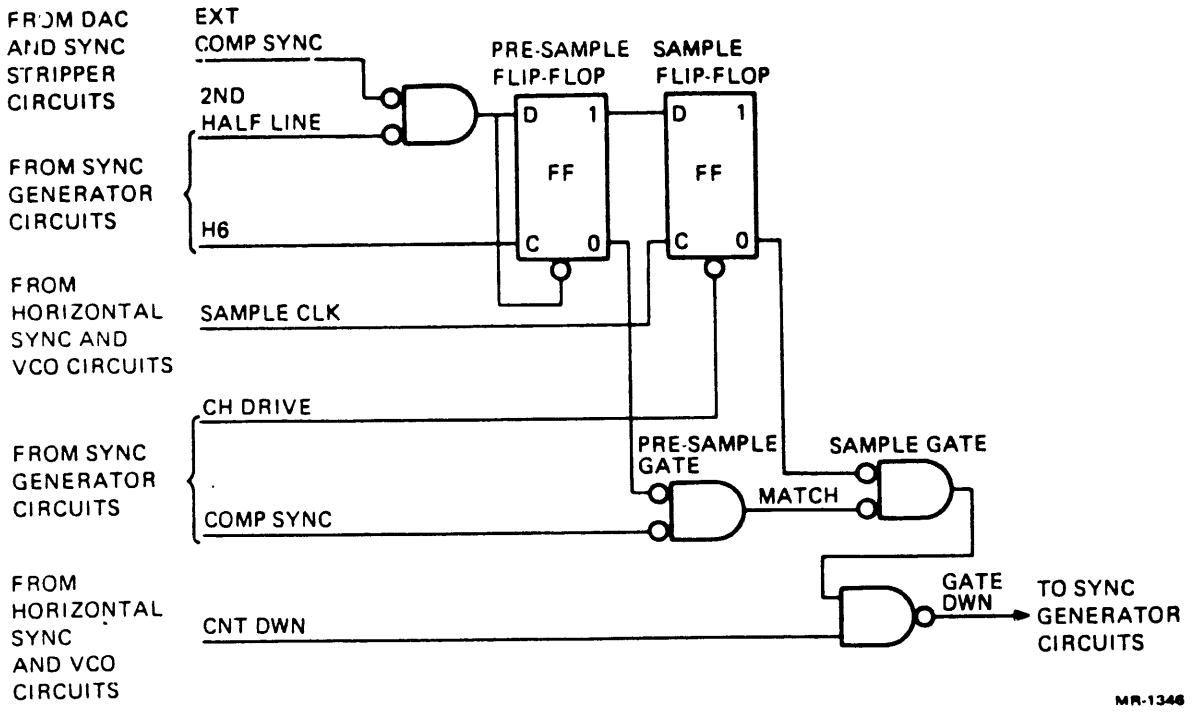


Figure 6-9 M7061 Vertical Sync Circuits -- Detailed Diagram

The "1" output from the Pre-Sample flip-flop drives the "D" input of the Sample flip-flop, while the "0" output is applied to the Pre-Sample NAND gate. When COMP SYNC is asserted (during vertical retrace), a Match condition is gated to one input of the Sample gate. At this time SAMPLE CLK from the Horizontal Sync and VCO circuits clocks the Sample flip-flop. The Sample flip-flop sets, providing an input to the Sample gate and reestablishing the sample window. The sample window is lost during the time the Pre-sample flip-flop is set and when Match is generated. This is due to the phase shift between EXT COMP SYNC and COMP SYNC. To compensate for this, the Sample flip-flop is used and clocked with SAMPLE CLK. SAMPLE CLK occurs within the retrace interval and provides enough time for EXT COMP SYNC and COMP SYNC to become phase matched. At the Pre-Sample gate, the state of Match is compared to the zero output from the Sample flip-flop. If a match is sensed during sample time, gate down (GATE DWN) remains high and no further action takes place. This indicates that the vertical counters are synchronized to the incoming EIA RS-170 sync signal. On the other hand, if Match is not true at sample time, GATE DWN goes low after count down (CNT

DWN) goes high. A low to high transition of GATE DWN causes the vertical counters in the Sync Generator circuits to count down. The counters will continue to count down until the output of the Sample flip-flop goes to the "1"state. When this happens a match occurs and GATE DWN goes high The sample window is terminated when CH DRIVE from the Sync Generator is negated. This occurs just before half-line time. Several samples may take place before synchronization occurs.

A sample is performed three times during each field. Successive samples and non-matches will ultimately count the vertical counters down until a match is obtained. Thereafter, successive samples will no longer cause a count down once a full vertical retrace interval match is obtained. Figure 6-10 shows the relationship between the sample times and the EXT COMP SYNC signal.

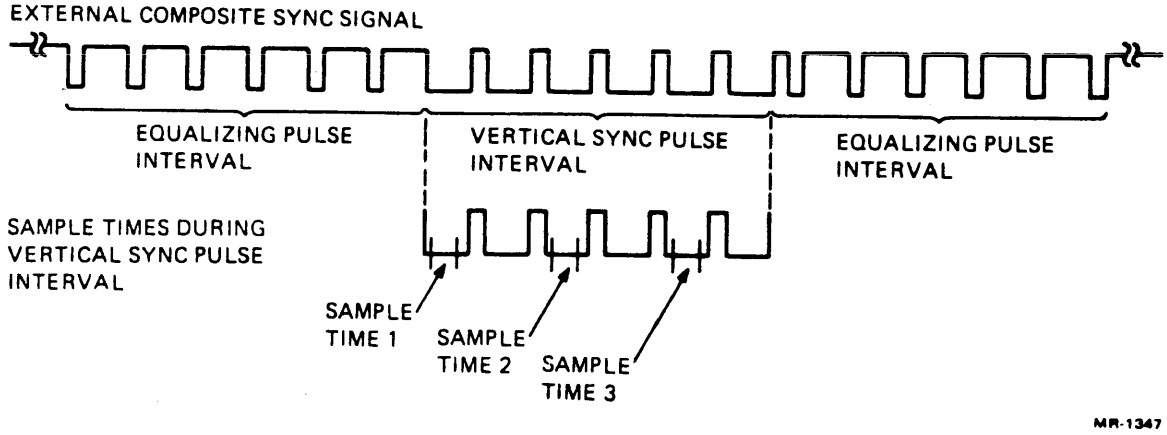


Figure 6-10
Vertical Sync Sample Times

6.3.6 Cursor Control Circuits

The Cursor Control circuits perform the following functions:

1. Calculate the X-Y position of the cursor crosshairs for display on the system monitor.
2. Control the intensification (on/off) of the crosshairs.
3. Convert the position of the joystick lever to a variable clock which is used to clock a counter for calculating the X-Y joystick positions.

4. Decode the joystick channel address provided by the Display Processor when M7061 registers are being accessed.

5. Read the cursor X-Y position to the Display Processor.

6. Generate the Joystick Switch interrupt.

7. Generate the Cursor Match interrupt.

8. Load the Cursor X-Y position from the Display Processor.

A discussion on each of these functions is included in the following paragraphs.

6.3.6.1 Control ROM And X-Y, Delta-Y Memory Logic -

Sheet 1 of Figure 6-11 illustrates the Cursor Control ROM and X-Y, Delta-Y Memory logic. This logic uses an X-Y, Delta-Y Counter (hereafter referred to as the counter) and a 4-word by 12-bit memory (X-Y, Delta-Y Memory -- hereafter referred to as the memory) for calculating the X-position and Y-position of the crosshairs, and for counting horizontal lines (Delta-Y) for intensifying the Y-crosshair. Each previous X, Y, or Delta-Y calculation is stored in the memory, then loaded into the counter and counted up or down for the new X-position, Y-position, or Delta-Y calculation (Delta-Y is always counted up). The new calculations are then stored in the memory for use during the next calculations. X, Y, and Delta-Y have separate locations in the memory.

The control function for the Cursor Control circuits is performed by the Control ROM, Latch A, the ROM Address Control, the 4:1 MUX (multiplexer), and the ROM Address Counter. Two routines are stored in the Control ROM. One routine is the calculating routine (ROM locations 00 through 17) and is used for calculating the X-Y joystick positions. The second routine is a draw routine (ROM locations 20 through 37) for drawing the crosshairs on the system monitor. The calculating routine is performed during vertical retrace time when vertical blanking is true (low). The draw routine is performed during active monitor display time. Entrance to the calculating and draw routines are controlled by ROM MSB (derived from V BLANK) and ADR CLK from the ROM Address Counter.

These signals control the address inputs to the Control ROM. When ROM MSB is low the calculating routine is entered. The draw routine is entered when ROM MSB is high. Sequencing within each routine is controlled by the ROM Address Control lines from the Control ROM to the ROM Address Control.

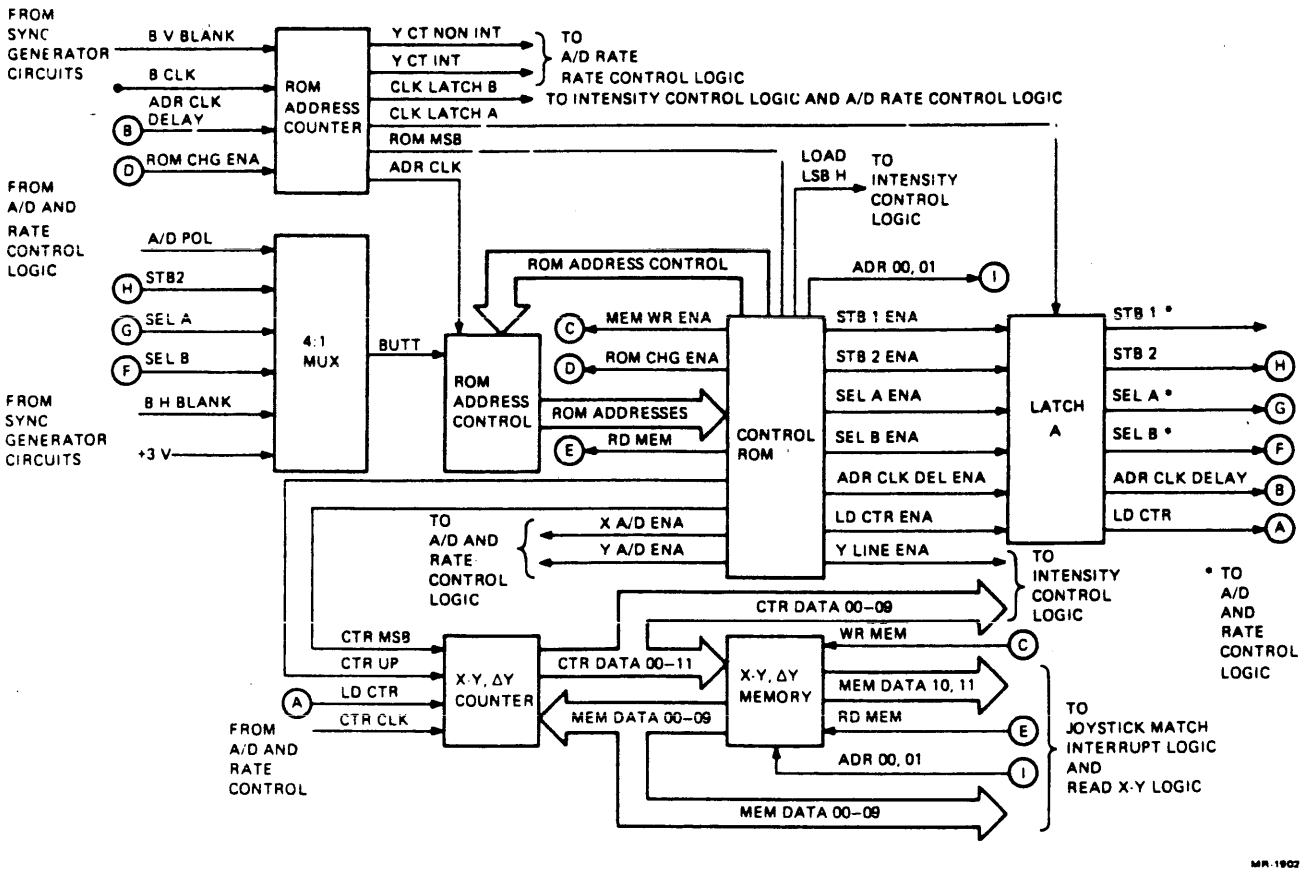


Figure 6-11
M7061 Cursor Control Circuits
(Control ROM and X-Y, Delta-Y Memory Logic) --
Detailed Diagram (Sheet 1 of 6)

When calculating the X-Y joystick positions, the ROM program monitors the polarity of the voltage from the joystick by sampling the A/D POL input to the 4:1 MUX. The BUTT output from the MUX controls the LSB of the ROM address for branching within the calculating and draw routines. If A/D POL is low (joystick moving to the right or up direction), the calculating routine sets the counter to count up. Conversely, A/D POL high (joystick moving to the left or down direction) sets the counter to count down. The CTR UP and CTR MSB signals from the Control ROM determine the counter direction. At the completion of vertical blanking time [B V BLANK L false (high)], ADR CLR and ROM CHG ENA cause the Control ROM MSB to change, thus entering the draw routine.

During X-Y calculations, the previous X-position is read from the memory to the counter. The counter is then set to count either up or down depending on the direction the joystick is being

moved. CTR CLK now clocks the counter for 300 uS. When the counter is stopped, it contains the new X-position of the joystick. This new X-position is then written to the memory for storage, replacing the previous X data, and is used during the next X-position calculation. Next, the previous Y-position is read from the memory to the counter. Again, the counter is set to either count up or down depending on joystick movement. The counter is again clocked for 300 uS and stopped. At the end of the count, the new Y-position is written to the memory for storage and used during the next Y-position calculation.

The X-Y, Delta-Y counter and X-Y, Delta-Y memory are also used to calculate which system monitor raster line is to be intensified for the display of the horizontal (Y) crosshair. For this calculation, Delta-Y from the memory is counted up until the count equals the raster line that is to be intensified. In essence, the counter is counting horizontal blanking pulses which occur at the end of each raster line. Delta-Y is therefore incremented as raster lines are traced on the system monitor. The count (CTR DATA 00-09) from the counter is applied to the Intensity Control logic (sheet 2) to intensify the raster line.

6.3.6.2 Intensity Control Logic -

Figure 6-11, sheet 2, shows the Intensity Control logic. The X-Y, Delta-Y Counter data (CTR DATA 00--09) is applied to the Y-Line Draw Control ROM. This ROM is programmed with the maximum number of visible raster lines for a VSV11/VS11 system monitor. Visible raster line maximums are: 480 for 60 Hz, 512 for 50 Hz. The maximum raster line number for the Y-Line Draw Control ROM is selected by the B ODD FRAME L, NON INT, and 50 Hz inputs to the ROM. When Delta-Y data (CTR DATA 00-09) matches the raster line count stored in the Y-Line Draw Control ROM, the ROM output goes low. Delta-Y LINE ENA is applied to Latch B and the latch is clocked (CLK LATCH B). The low output from Latch B enables a NAND gate, the output of which sets the H-Line flip-flop. The output of the H-Line flip-flop is applied to a NAND gate. If the Crosshair Enable flip-flop has been set by Joystick Status instruction bits 04 and 05 (Crosshair Intensity and Crosshair Intensity Enable, respectively -- refer to Chapter 3) JSV DATA will be applied to the Sync Generator DACs for one raster line. Thus, one raster on the system monitor will be intensified. The intensified raster line is the horizontal line of the crosshair. At the end of the raster line B H BLANK goes low and clocks the H-Line flip-flop to the reset state. If the small cursor is selected, the H-Line flip-flop is gated with the counter. JSV DATA is enabled for 17 pixel positions when the counter reaches 8 pixel positions before the crosshair position.

The vertical (X) crosshair results from gating Delta-X RIPPLE CLK through the NAND gate. This pulses JSV DATA low once for each raster line. Thus, the vertical crosshair is a series of vertical intensified spots on the system monitor. As with the

horizontal crosshair, the Crosshair Enable flip-flop must be set and B H BLANK L and B V BLANK L must be high to enable the AND gate. If the small cursor is selected, Delta-X RIPPLE CLK is gated with a flip-flop which is set when Delta-X is eight raster lines of the horizontal crosshair position.

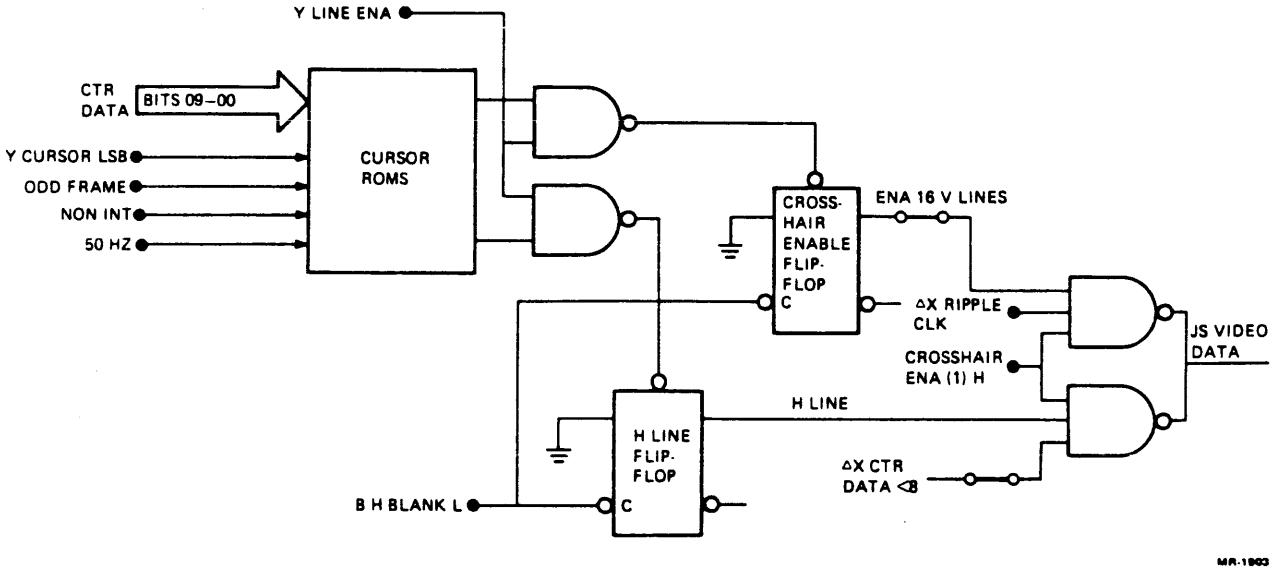


Figure 6-11
M7061 Cursor Control Circuits
(Intensity Control Logic) --
Detailed Diagram (Sheet 2 of 6)

6.3.6.3 A/D Rate Control Logic -

The A/D Rate Control logic is shown on sheet 3 of Figure 6-11. This logic converts the analog voltage from the joystick into a digital clock for the X-Y, Delta-Y counter on sheet 1. The clock rate varies with the amount of joystick movement.

When calculating the X-crosshair position, the Control ROM asserts X A/D ENA. B ODD FRAME L from the Sync Generator circuits is always high in Non-Interlaced mode. These two signals are gated to produce RUN X A/D which enabes X IN to the analog switch, and also enables the Divide-By-16 counter. X IN, which can vary from +1 V to -1 V, depending on the joystick position, passes through the Analog Switch and is applied to the Absolute Value Converter. From the X or Y input, the Absolute Value Converter produces A/D POL which indicates the direction in which the joystick is moved. A/D POL is applied to the 4:1 MUX on sheet 1 to control the LSB of the Control ROM address. The +1 V to -1 V X or Y input to the Absolute Value Converter is converted to a voltage from 0 V to 4 V at the converter output. This voltage is applied to a timer which produces A/D CLK. The number of A/D CLK pulses varies according to joystick movement. From the timer, A/D CLK is applied to the Divide-by-16 counter which has been enabled by RUN X A/D. This counter divides A/D CLK by 16 and applies it through an OR gate to the 4:1 MUX. The dividing of A/D CLK is necessary to produce the proper clock rate for the X-Y, Delta-Y counter on sheet 1 when calculating X- or Y-crosshair positions. The Y IN input from the joystick is handled by the A/D and control logic in a manner similar to that just described for the X IN input. RUN Y A/D selects the Y IN input and enables the Divide-by-16 counter.

The X-Y, Delta-Y counter on sheet 1 is clocked by CTR CLK from the 4:1 MUX (sheet 3). Three different clocks (CTR CLK) can be applied to the counter, depending upon the type of calculation (X, Y, or Delta-Y) being performed. The 4:1 MUX selects these clocks and applies them to the counter via the CTR CLK line. When calculating X- or Y-crosshair positions, the X-Y CLK from the Divide-by-16 counter is selected. When drawing the X-crosshair (vertical), B CLK is selected, as this clock is used to clock pixels to the system monitor. The vertical crosshair is actually intensified pixel positions. During the drawing of the Y-crosshair, horizontal blanking pulses are counted. Horizontal blanking is the Y CNT input to Latch B. Y CNT is counted twice for each frame. This provides positioning of the horizontal crosshair within the proper frame.

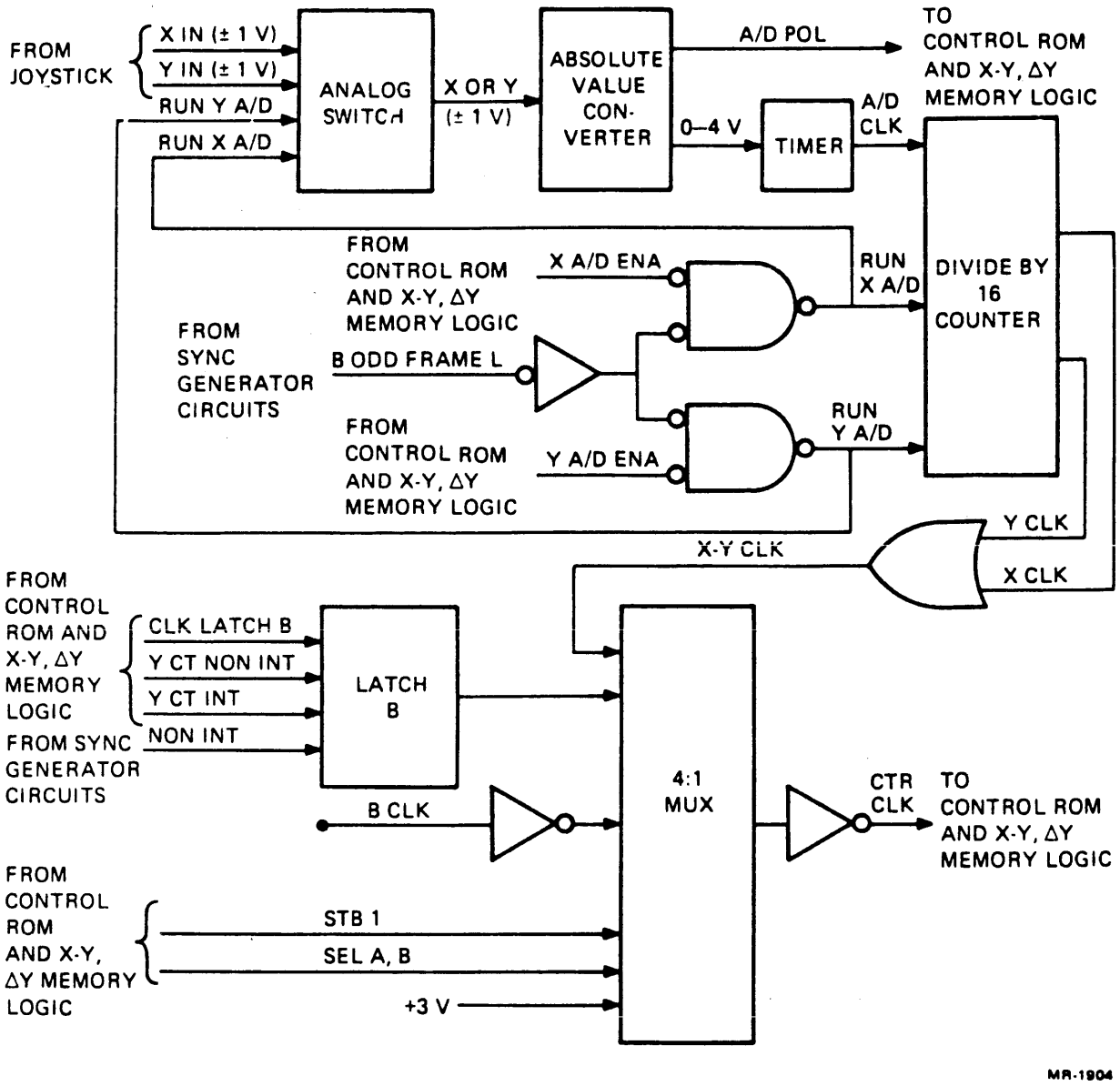


Figure 6-11
M7061 Cursor Control Circuits
(A/D Rate Control Logic)
Detailed Diagram (Sheet 3 of 6)

6.3.6.4 Joystick Address Decode/Switch Interrupt Logic -

The Joystick Address Decode/Switch Interrupt logic decodes the joystick address for joystick selection and generates the Switch interrupt to the M7064 Display Processor when the joystick switch is pressed.

Sheet 4 of Figure 6-11 illustrates the Joystick Address Decode/Switch Interrupt logic. Four joysticks can be accomodated by the VSV11/VS11 system if four M7061 Sync Generator/Cursor Control modules are used. Each joystick has a unique address. These addresses are encoded in bits 08 and 09 of the Joystick Status instruction and are applied to the M7061 by the Display Processor via DBUS Data bits 10 and 11. Joystick address decoding is accomplished on the M7061 module and is set up by jumpers W5, W6, W7, and W8. The joystick addresses and the jumper configurations are as follows:

Joystick Addresses	Jumpers W5	W6	W7	W8
00	OUT	IN	OUT	IN
01	OUT	IN	IN	OUT
02	IN	OUT	OUT	IN
03	IN	OUT	IN	OUT

A system with one joystick has its address at 00. When the proper joystick address is placed on the DBUS (bits 10 and 11) and decoded along with JS STATUS from the D SEL Line Decoder on sheet 5, INTR CLR is applied to other M7061 modules in the system to prevent them from generating other joystick interrupts. STAT CLK clocks all the M7061 status flip-flops. The Switch Enable flip-flop is set when DBUS 00 and 01 (Switch Interrupt Enable and Switch Interrupt bits, respectively of the Joystick Status instruction) are asserted and when STAT CLK clocks the flop. When the Switch Enable flip-flop is clocked, DBUS 00 is stored. Now, when the joystick interrupt switch is pressed, JS SWITCH goes low. This gates the zero output of the Switch Enable flip-flop to the Switch Interrupt flip-flop, thus setting the Switch Interrupt flip-flop. When the Switch Interrupt flip-flop sets, JS SWITCH INTR is sent to the Display Processor via the DBUS. Only one switch interrupt can be generated as the Switch Interrupt Enable flip-flop is automatically reset after the first interrupt is produced. This prevents multiple interrupts from occurring if the joystick interrupt switch is pressed more than once. A new switch interrupt can only be initiated if another Joystick Status instruction enables it again.

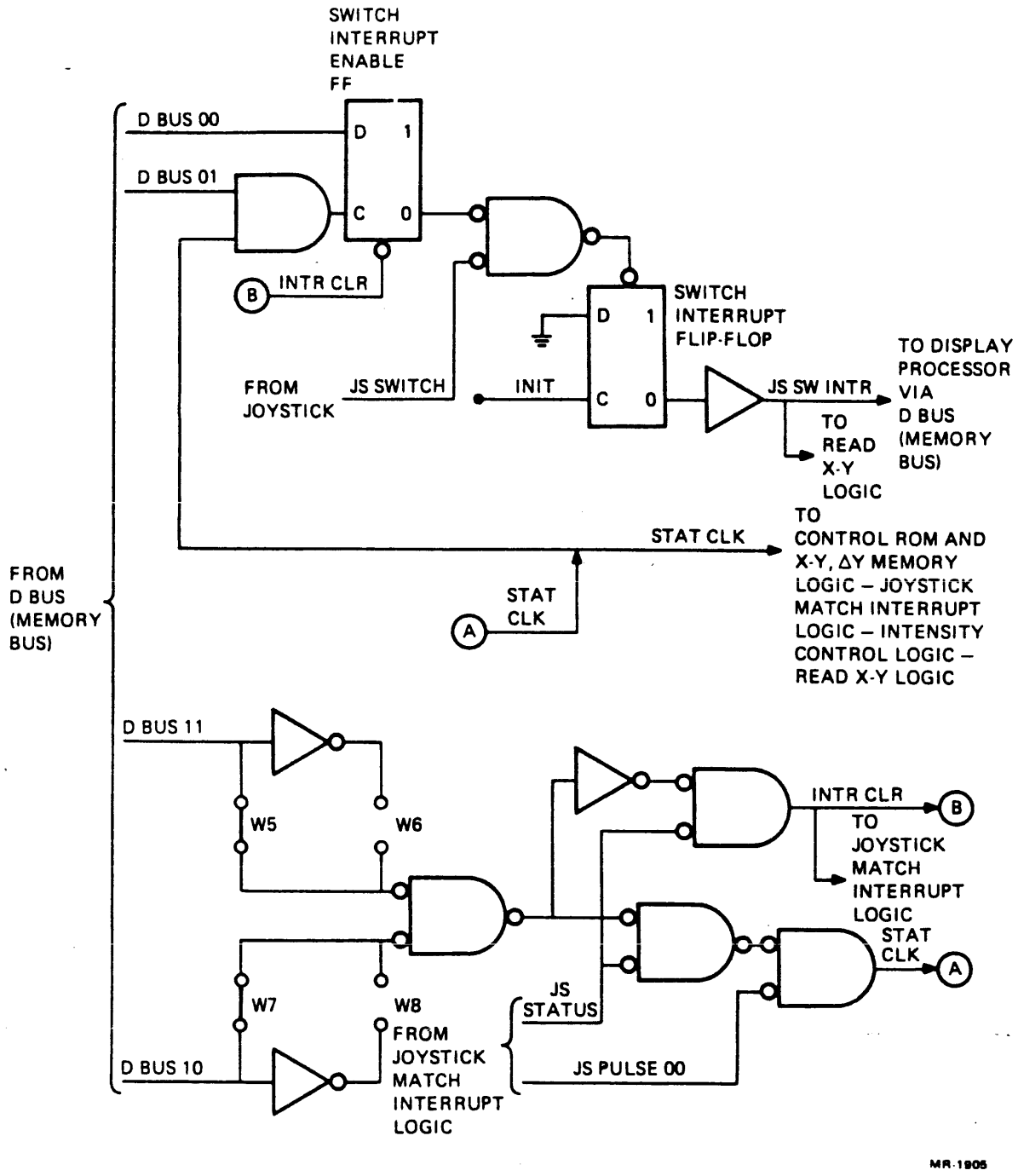


Figure 6-11
M7061 Cursor Control Circuits
(Joystick Address Decode/Switch Interrupt Logic) --
Detailed Diagram (Sheet 4 of 6)

6.3.6.5 Read X-Y Logic -

The cursor position stored in the X-Y Memory (sheet 1) can be read by the Display Processor through the Joystick Status instruction, or when the joystick interrupt switch is pressed. Sheet 5 of Figure 6-11 illustrates the M7061 Read X-Y logic.

When the Joystick Switch interrupt (JS SW INTR) is generated, the Display Processor responds with a request for the cursor coordinates. JS SW INTR, D SEL 00--03, and D PULSE are decoded to produce READ ENA, which presets the Read flip-flop. This produces READ (1) L which enables the READ X and READ Y AND gates and the 3-state drivers. Next, SEND X is produced (sheet 6) as the result of decoding the RD X CUR command from the D SEL lines from the Display Processor. SEND X is gated with READ (1) L and is clocked into the Data Ready flip-flop with B CLK. When the Data Ready flip-flop sets, DATA RDY is sent to the Display Processor. Meanwhile, READ (1) H causes the Control ROM (sheet 1) to read the X-position data out of the X-Y, Delta-Y Memory (sheet 1) onto the MEM DATA 00--09 lines to the 3-state DBUS drivers. The 3-state drivers then transfer the X-position data to the Display Processor via the DBUS.

When the X-position data is stored in the Display Processor, the processor encodes the D SEL lines (sheet 6) with a RD Y CUR command to read the Y cursor position data. The Data Ready flip-flop is again set, generating DATA RDY. SEND Y causes the Control ROM to read Y-position data from the X-Y, Delta-Y Memory to the 3-state drivers and to the Display Processor.

The X-Y joystick position can also be read by the Display Processor via the issuance of the Joystick Status instruction. A Joystick Switch interrupt is not required. This read occurs when the Display Processor sets DBUS 06 to a one (DBUS 06 is the result of bit 06 of the Joystick Status instruction). DBUS 06 is gated with READ (1) L which is in the zero state at this time. The Read flip-flop sets when clocked by CLK READ, which is the NOR gate output of STAT CLK. SEND X or SEND Y causes DATA RDY and the transfer of the X- or Y-position data from the X-Y, Delta-Y Memory to the Display Processor as previously explained for the JS SW INTR read.

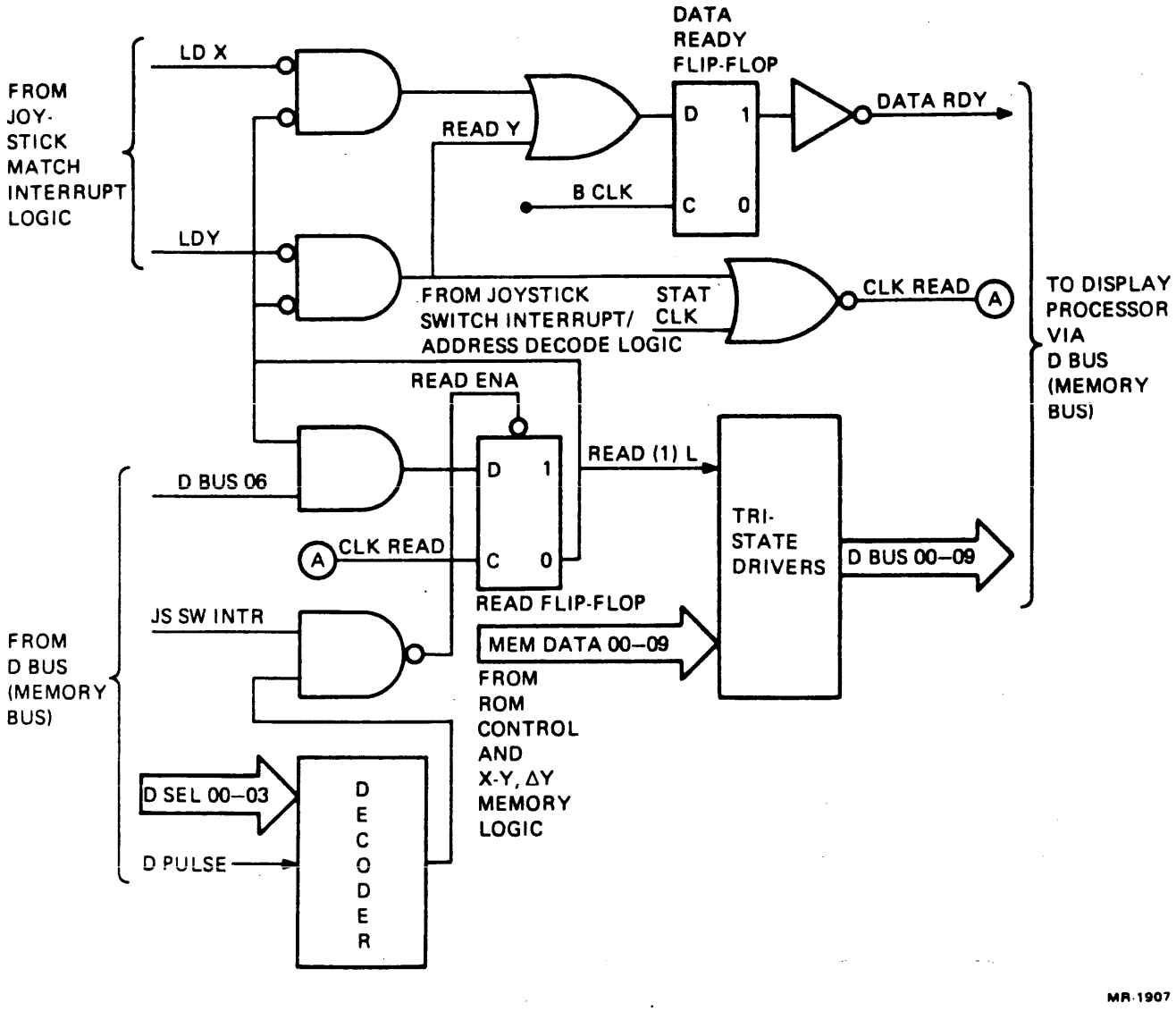


Figure 6-11
M7061 Cursor Control Circuits
(Read X-Y Logic) --
Detailed Diagram (Sheet 5 of 6)

6.3.6.6 Joystick Match Interrupt Logic -

The Joystick Match Interrupt logic (sheet 6 of Figure 6-11) produces the Joystick Match interrupt (JS MATCH INTR) when the joystick position (X and Y) matches a pixel location which is being written into the Image Memory by the Display Processor at the time the joystick interrupt switch is pressed. The interrupt occurs if the Match Enable flip-flop is set by a Joystick Status instruction. STAT CLK is gated with DBUS 03 (Match Interrupt Enable bit) to clock DBUS 02 (Match Interrupt) to the Match Enable flip-flop. The Match Enable flip-flop sets, enabling a NAND gate. When the joystick switch is pressed the comparators are enabled.

Meanwhile, the Control ROM (sheet 1) causes the X-Y Delta-Y Memory to place X-position data on the MEM DATA 00-11 lines to the comparator. DBUS 00-11 lines to the comparator have X position of the pixel data written to the M7062 Image Memory by the Display Processor at this time. If the data on the MEM DATA lines compares with the data on the DBUS lines, the comparator produces MATCH. Since the first compare compares for an X-match, MATCH is clocked into the X-Match flip-flop by LD X. The X-Match flip-flop stores the condition of the X-Match.

When X matches, the Control ROM (sheet 1) causes the X-Y, Delta-Y Memory to place Y-position data on the MEM DATA 00--11 lines. At this time, the DBUS 00-11 lines have the Y-position of the pixel data which is being written to the Image Memory by the Display Processor. Again, a MATCH occurs when the data on the MEM DATA lines matches the data on the DBUS lines. This time the MATCH is for the Y-position and it is clocked into the Y-Match flip-flop with LD Y. When the Y-Match flip-flop sets, JS MATCH INTR L is sent to the Display Processor. The Match Interrupt logic seeks a match as long as the joystick interrupt switch is pressed. The interrupt is cleared when MATCH ENA goes low.

6.3.6.7 Load X-Y Logic -

The X-Y Memory can be written into by the Display Processor. D SEL 00--03, D PULSE 00, and ADDR MATCH produce WRT X or WRT Y. Either signal will force the Control ROM into address zero and select PROM E19 instead of E29. The data is taken from the DBUS and loaded into the counter. Then it is transferred into the X-Y Memory and the DATA READY signal is sent to the Display Processor, indicating the data is stored and ready. The Display Processor encodes a zero on the D SEL 03-00 lines and enables the D PULSE to the Control ROM to transfer the data.

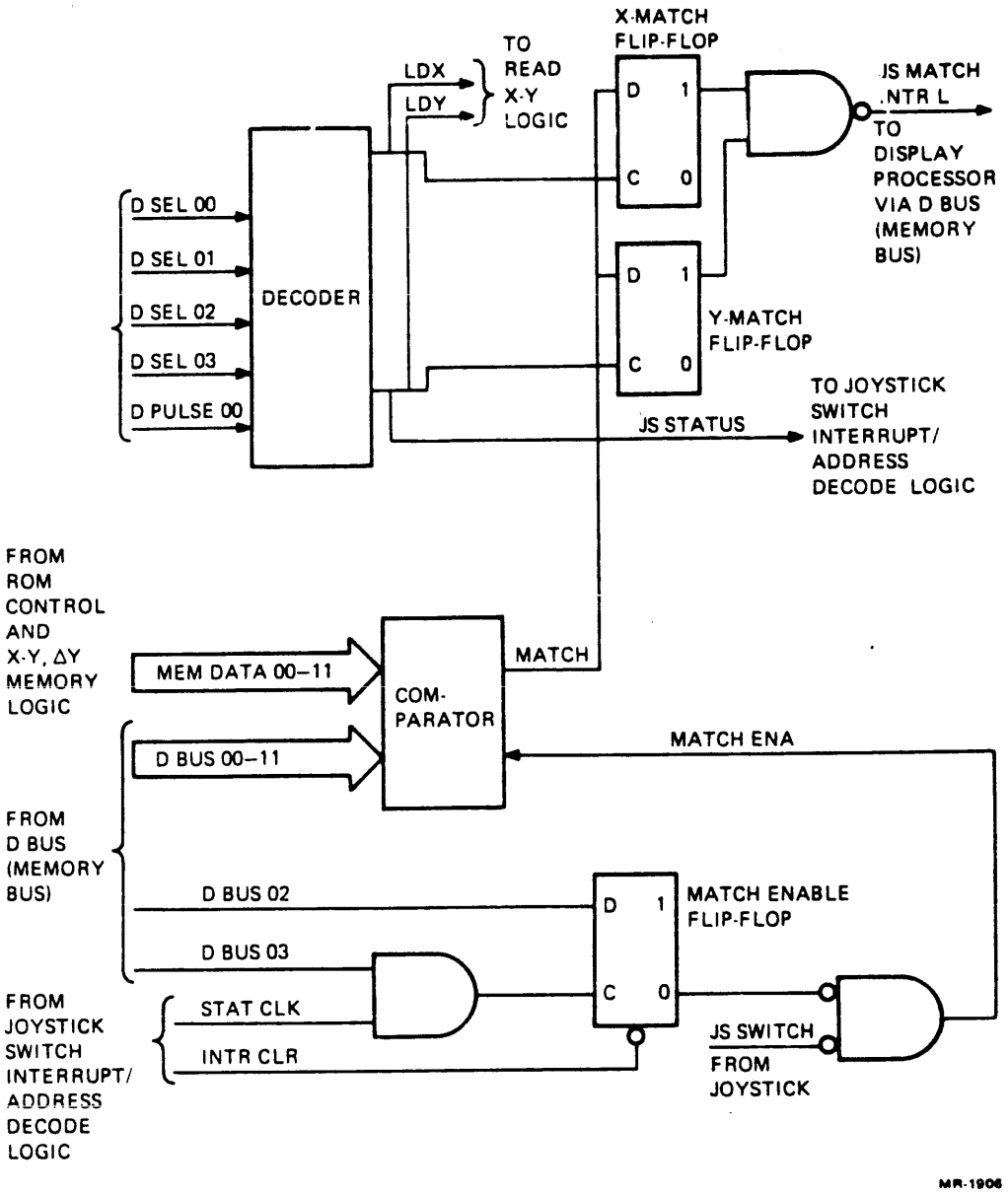


Figure 6-11
M7061 Cursor Control Circuits
(Joystick Match Interrupt Logic) --
Detailed Diagram (Sheet 6 of 6)

6.3.7 H3060 Joystick

The H3060 Joystick is supplied with VSV11/VS11 systems using the M7061 Sync Generator/Cursor Control module. The Joystick consists of two 5K ohm potentiometers (Figure 6-12) mounted at right angles and mechanically coupled to the joystick control

lever with a gimbal coupling. The gimbal coupling transfers movement of the joystick control lever to the X- and Y-position potentiometers. Joystick control lever movement in only the X-direction only affects the X-position potentiometer; the same is true for movement in the Y-direction affecting the Y-position potentiometer. Both potentiometers are affected by equal amounts when the joystick control lever is moved at a 45 degree angle from its center position.

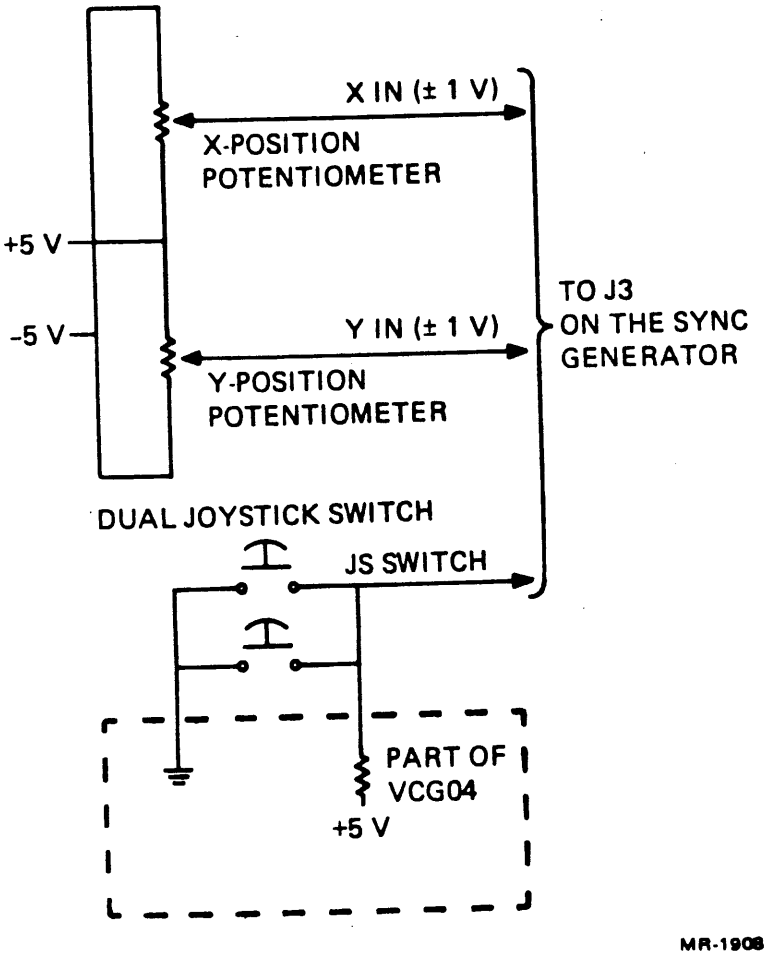


Figure 6-12
H3060 Joystick Circuits

Each potentiometer has 10 V (+5 V and -5 V) across it. The output of each potentiometer can vary from +1 V to -1 V, depending on the amount of joystick control lever movement. When the joystick control lever is centered both potentiometers are centered and their outputs are zero. The joystick control lever is spring-loaded to the center position. Trim tabs are provided to allow "trimming" of the potentiometers at the center position. If the potentiometers are not centered when the joystick is released, the vertical or horizontal crosshair (or both, depending on which potentiometer is out of calibration) will

drift. Vertical crosshair drift is compensated by adjusting the trim tab located in the vertical slot towards the right of the joystick control unit until movement of the crosshair stops. Drift of the horizontal crosshair is offset by the trim tab located in the horizontal slot just below the joystick control lever.

In addition to the joystick control lever, the H3060 Joystick has dual interrupt switches. These switches are located under pads on each side of the joystick control lever and are used to produce the Switch and Match interrupts. The switches are wired in parallel and control the JS SWITCH signal to the Sync Generator module. Normally, JS SWITCH is pulled to +5 V through a resistor on the Sync Generator module. When either switch is pressed, JS SWITCH is grounded (active state) until the switch is released.

The H3060 joystick is equipped with an eight-foot (2.29 meters) cable. This cable connects to a 20-foot (5.7 meters) cable (part number 7015822 supplied with the Sync Generator and joystick) which in turn connects to J3 on the Sync Generator module. The Sync Generator supplies operating voltages and a ground for the Joystick.

6.3.8 5 V Converter

The Sync Generator DAC and Sync Stripper circuits use -5 V in addition to the normal +5 V. A dc-to-dc inverter (not illustrated) is used to convert +5 V to -5 V. The inverter is comprised of a transistor multivibrator using a saturable transformer, a negative diode rectifier, and an L-C filter. A three-terminal regulator produces regulated -5 V for the DAC and Sync Stripper circuits as well as the M7062 Image Memory module.

6.3.9 Video Bus

The Video Bus is a bus structure which provides an interconnection scheme between any two successive C-D slots on an H9273 type backplane. Interconnections are wired daisy-chain fashion from side two of the first slot to side one of the second slot, and from side two of the second slot to side one of the third slot. This pattern repeats for all nine C-D slots of an H9273 type backplane.

Modules designed to function together as module sets (such as the M7064, M7061, and M7062) are inserted into the C-D slots of an H9273 type backplane. The Video Bus implemented on this C-D Interconnect provides for the exchange of data and control signals between modules in the VSV11 module set.

There can be up to 33 signals on the Video Bus. These signals are broken down into three broad categores:

1. Video data

2. Timing and Synchronization

3. Spares

For the M7061, the video data (V DATA 00-07) lines consist of eight Video Bus lines. These lines are driven by the Image Memory module and are terminated at the Sync Generator. Timing and synchronization lines for the Sync Generator consist of B CLK, B ODD FRAME, B V BLANK, B H BLANK, B H CLR, STALL, V H CLR, 50/60 Hz, and NONINTERLACE. These signals are generated by the Sync Generator and are driven down the Video Bus and terminated on the Display Processor module. In addition, the Sync Generator timing and synchronization lines are connected from side one to side two of the Sync Generator module. This allows these signals to be passed down the Video Bus by means of the daisy chain interconnections. Table 6-1 lists the Sync Generator finger connections and the associated signals. Note that except for DA1, DC1, DT1, and DV1, side one "D" fingers carry the same signals as side two "D" fingers. The "D" finger signals are the lines on the Video Bus which are daisy-chained through all modules on the bus and terminate at the Display Processor. On the other hand, Table 6-1 shows that the 8 video data lines (V DATA 00-07) are only connected to side two "C" finger pins. The video data lines are terminated on the Sync Generator and are not passed to other modules on the bus. Also, one Sync Generator only utilizes four video data lines. A minimum of two modules are required to make use of all the video data lines. However, a small graphic system may use only one Sync Generator module.

It was previously mentioned that the M7061, M7062, and M7064 are a graphic module set which are designed to function together over the Video Bus. These modules must be inserted into the Video Bus in a specified order. The specified order considers Video Bus modules as first, middle, and last modules. The first module is inserted into the first (lowest numbered) slot (not necessarily slot one) on the Video Bus. This module may or may not have signals on side one fingers since it is not required to pass signals to an adjacent module (module in first used slot minus one). However, signals on side two fingers of the first module are connected to the second module in the adjacent slot (first used slot plus one). In the M7061, M7062, M7064 module set, the M7061 module is classified as a first module.

Table 6-1
M7061 Finger Pin Assignments (See Note)

"C" Fingers (Side 1 -- Component Side)	Signal	"D" Fingers (Side 1 -- Component Side)	Signal
CA1	Not Used	DA1	Not Used
CB1		DB1	Not Used
CC1		DC1	Not Used
CD1		DD1	Not Used
CE1		DE1	B ODD FRAME
CF1		DF1	B V BLANK
CH1		DH1	B H BLANK
CJ1		DJ1	B H CLR
CK1		DK1	Not Used
CL1		DL1	Not Used
CM1		DM1	50/60 HZ
CN1		DN1	NONINTERLACE
CP1		DP1	B COMPOSITE SYNC
CR1		DR1	INIT H
CS1	Not Used	DS1	B CLK
CT1	GND	DT1	GND
CU1	Not Used	DU1	Not Used
CV1	Not Used	DV1	Not Used

NOTE

Except for the power and ground fingers, the "A" and "B" fingers of the Sync Generator module are unused.

Table 6-1 (Cont'd)
M7061 Finger Pin Assignments (See Note)

"C" Fingers (Side 2 -- Solder Side)	Signal	"D" Fingers (Side 2 -- Solder Side)	Signal
CA2	+5 V	DA2	+5 V
CB2	Not Used	DB2	Not Used
CC2	GND	DC2	GND
CD2	Not Used	DD2	Not Used
CE2	V DATA 0	DE2	B ODD FRAME
CF2	V DATA 1	DF2	B V BLANK
CH2	V DATA 2	DH2	B H BLANK
CJ2	V DATA 3	DJ2	B H CLR
CK2	V DATA 4	DK2	STALL
CL2	V DATA 5	DL2	Not Used
CM2	V DATA 6	DM2	50/60 HZ
CN2	V DATA 7	DN2	NONINTERLACE
CP2	V DATA 8	DP2	B COMPOSITE SYNC
CR2	JS DATA	DR2	INIT H
CS2	Not Used	DS2	B CLK
CT2	Not Used	DT2	Not Used
CU2	-5 V	DU2	Not Used
CV2	MEM STOP	DV2	Not Used

NOTE

Except for the power and ground fingers, the "A" and "B" fingers of the Sync Generator module are unused.

A middle module is a module that communicates with the preceding and next modules in the module set. This module has fingers on side one connected to fingers on side two to allow signals to pass down the Video Bus to the last module. If the M7061 is the first module, synchronization and timing signals generated on the M7061 are passed to the middle module (M7062 Image Memory). The middle module, in turn, passes the synchronization and timing signals to the last module (M7064 Display Processor). In the M7061, M7062, M7064 module set, the M7062 image memory module is classified as a middle module.

The last module can only communicate with the modules preceding it. As its name implies, the last module is the last module on the Video Bus (not necessarily the last slot) and has bus interconnects only on the side one fingers. Side two fingers may have signals which are used for testing or other purposes, but these signals are not connected to the Video Bus. In the M7061, M7062, M7064 module set, the M7064 Display Processor module is classified as a last module.

Thus far, only a basic graphic system consisting of a M7061, M7062, M7064 module set has been considered. A larger graphic system may have up to four each of M7061 and M7062 modules and one M7064 module. For this system, the M7064 is still the last module, and one M7061 module is the first module. The M7061 selected for use as the first module would have an active Sync Generator. This M7061 can be considered as the master M7061. The remaining three M7061 modules have their Sync Generator circuits disabled (by means of a switch on the M7061) and are then classified as middle modules along with the M7062 modules. Only the DAC and Cursor Control circuits in these M7061s are used. This graphic system would be a system using all nine video bussed C-D slots on an H9273 type backplane. The M7064 module (a last module) would occupy slot nine; slots eight, six, four, and two would contain M7062 modules (middle modules), while slots seven, five, and three would contain M7061 modules (middle modules) with disabled Sync Generator circuits. Slot one would contain the M7061 module (first module) with the active Sync Generator circuits. This typical graphic system could operate four monitors. Note that in this system each M7062 is paired with a M7061. Whenever a M7062 Image Memory module is used, one M7061 Sync Generator module must be used along with it. However, a graphic system only requires one active Sync Generator to supply synchronization and timing. The paired M7061 and M7062 modules only use the DAC circuits on the M7061 module.

CHAPTER 7

MAINTENANCE

7.1 INTRODUCTION

The maintenance philosophy for the VSV11/VS11 is corrective maintenance by replacing a failing module (M7064 Display Processor, M7062 Image Memory, M7061 Sync Generator/Cursor Control, or monitor module) or an assembly (Cable, Joystick). System failures are uncovered by running the DEC/X11 System Exerciser (for PDP-11) or the VS11 Level 2 Diagnostic (for VAX). If the running of these programs points to a failing VSV11/VS11 unit, the VSV11/VS11 standalone diagnostic is then run to aid in determining which module or assembly within the VSV11/VS11 is failing. A failing module or assembly can be isolated with the aid of the troubleshooting tables provided in this chapter.

There are no preventive maintenance procedures or periodic alignment or adjustment procedures for the VSV11/VS11.

7.2 TOOLS AND TEST EQUIPMENT

The only tools required to maintain the VSV11/VS11 are an oscilloscope (such as a Tektronix 485), a logic probe, a Volt-Ohm-Milliammeter (VOM), and a small common-blade screwdriver suitable for making potentiometer adjustments. With the exception of the oscilloscope, these tools are contained in the DIGITAL Field Service Tool Kit.

7.3 TEST PROGRAMS

7.3.1 DEC/X11 System Exerciser

A DEC/X11 module is supplied for using the VSV11/VS11 graphics option with PDP-11 and LSI-11 systems. Running DEC/X11 will aid in determining a failing option (such as the VSV11/VS11) but may not aid in option repair. Option fault isolation can be determined through use of the specific option diagnostic. Refer to the instructions supplied with the DEC/X11 module for running the VSV11/VS11 within the DEC/X11 System Exerciser.

7.3.2 VAX/VMS Level 2 Diagnostic

The program EVTCA is provided for use on VAX-11 systems in order to aid in finding system problems and to allow on-line testing. It is a subset of the standalone program EVTCB, described in Paragraph 7.3.3. It runs under the VMS operating system with the VS11 driver. If problems are encountered when running this program, note the symptom and then use the standalone diagnostic EVTCB to isolate the cause.

7.3.3 VSV11/VS11 Option (Standalone) Diagnostics

The program CVVSA is supplied for use on PDP-11 and LSI-11 systems; the Level 3 program EVTCB is supplied for use on VAX systems. These programs are nearly identical, differing only in the format of error reports and operator dialog. In the discussions which follow, therefore, they will be referred to merely as "the diagnostic".

The diagnostic consists of 35 tests which exercise the VSV11 or VS11 graphics option. These tests make use of the complete VSV11/VS11 instruction set to determine whether or not the M7064 Display Processor module, the M7062 Image Memory module(s), and the M7061 Sync Generator/Cursor Control module(s) are functioning properly.

Tests 1 through 22 verify M7064 Display Processor operation; this set of tests is termed the "DPU-Only" set because they can be run without communication with the M7061 and M7062 over the DBUS Cable (all modules must, however, be plugged into the backplane). Test 23 verifies the M7061 Sync Generator/ Cursor Control module together with the M7064 Display Processor. Tests 24 through 27 further test the M7064 Display Processor but require communication with the Image Memory. Tests 28 through 30 test the M7062 Image Memory modules. Test 31 is not used; it is reserved for future expansion. Test 32 is a visual display using most of the VSV11/VS11 instruction set. Test 33 verifies operation of the Joystick unit together with the cursor control and interrupt circuits on the M7061. Test 34 provides various

displays (crosshatch, color bars, etc.) for use in adjusting display monitors connected to the VSV11/VS11 system. Test 35 is a "Configuration Typeout" routine which prints out on the console terminal the Image Memory and Sync configuration (i.e., number of memory and sync channels, number of bits in each memory, and scanning mode).

Tests 1 through 32 can be run automatically in sequence, with individual test failures (errors) indicated on the console terminal (not the VSV11/VS11 graphics monitor). Any test can also be called up and run individually. Tests 33 through 35 are always "standalone" tests and cannot be run with other tests selected.

After the diagnostic is loaded and running, no operator intervention is required beyond the initial start-up dialog (selection of units, etc.). Operator intervention is only required to call up and run the "standalone" tests.

As the diagnostic runs, some of the tests provide visual patterns on the graphics monitor. Observation of these patterns is necessary to verify operation of circuits which are inaccessible to the program.

Refer to the diagnostic listing for details on loading and running the diagnostic and for a description of each test.

7.4 FAULT ISOLATION (TROUBLESHOOTING)

Troubleshooting is carried out with the aid of the diagnostic program and the two Symptom/Cause/Corrective Action tables presented below. There are two basic classes of problems which can occur:

1. Program-detected faults, which result in an error report printout; use Table 7-1 to aid in isolating the fault.

2. Visually-detected faults, which do not result in an error report but cause a corrupt or non-existent display on the graphics monitor; Table 7-1 covers general video problems and can be used when a Monochrome monitor (VT100) is being used; if a Color monitor (VRV02) is being used, use Table 7-2 to aid in isolating video faults.

In the listing of problem symptoms in the tables, the causes and corrective actions are given assuming that no symptom appearing earlier in the table is present. Therefore, during troubleshooting always scan the appropriate table from the beginning.

When using the tables, refer to the diagrams in Chapter 2 for location of system components (switches, jumpers, potentiometers)

and proper setup of the switches and jumpers. Note that, in the tables, the word "potentiometer" is shortened to "pot". When dealing with the VRV02 monitor, refer to the Hitachi monitor manual. When dealing the the VT100, refer to the VT100 Technical Manual.

If, in the troubleshooting charts, it is indicated that a cable is to be disconnected, be sure to reconnect the cable before proceeding to another step. If a module is to be removed or swapped, make sure that power is OFF before action is taken. When disconnecting or connecting cables, it is not necessary to remove power. Note that, when referring to module pins (fingers), the pin number is given with respect to the module and not necessarily the backplane; ie., if the modules are installed in a DDV11 Hex-height backplane, module pins in the A through D slots appear as backplane slots C through F, respectively.

If several actions are listed for troublshooting a particular problem, stop after the step that appears to fix the problem. In all cases, after a problem is fixed, always run the entire diagnostic to make sure that other problems did not arise.

Before proceeding with troubleshooting, it is wise to verify that all proper voltages are present on the backplane (Paragraph 2.4). In addition, refer to Paragraph 7.5 for a procedure to assure proper quality of video output signal when using the VRV02-BA/BB monitor.

Note that backplane problems can cause a variety of failures, some of which masquerade as module problems. If the normal troubleshooting steps do not seem to isolate a problem to a particular component, suspect the backplane. In such cases, carefully inspect the backplane for broken or bent pins, broken wires and insulation, broken or shorted etch, solder splashes, and faulty connector slots. It may be helpful to remove all modules and vacuum and clean the connector slots.

Before replacing a defective module with one from spares, make sure that the switches and jumpers on the replacement module are configured like those on the faulty module (if the faulty module had indeed been working at one time). If there is doubt as to the correct settings of switches and jumpers, refer to the setup procedures in Chapter 2 and verify the settings.

Table 7-1
Basic Troubleshooting Chart

SYMPTOM	CAUSE(S)	CORRECTIVE ACTION
Bus Hung; Can't Boot System	Bad M7064 Display Processor	Replace M7064 (assumes system is OK without VSV11/VS11).
	Bad DW11 Unibus-to-LSI-11 Bus Converter (VS11)	Disconnect the cables from the M8217 module; replace M8217 if the problem persists. If disconnecting the cables fixes the problem, reconnect the cables to the M8217 and disconnect them from the M9403; if the problem persists, replace the cables. Remove the M9403 and reconnect the cables; if the problem persists, replace the M9403. Swap the M7064 and reinstall all modules; if the problem persists, inspect the backplane and replace it if necessary.
"Dead" VSV11/VS11 (Non-Existent device register)	Address switches on M7064 improperly set.	Verify settings of switches on DIP switch pack E31 of M7064.
	No Timing (VBUS signal B-CLK): Bad M7061 Sync Generator, backplane, or other module.	Verify, with oscilloscope or logic probe, that B-CLK (80 nS square wave) is present on pin DS1 of M7064 and DS2 of M7061 (FS1, FS2 if DDV11 backplane). If it is on neither pin and external sync is being used, verify that the external sync source is being applied to the M7061; adjust pot R48 on the M7061; if the problem persists replace the M7061. If the problem still persists, either the backplane is bad or one of the other modules is loading the signal. Remove all modules except M7061 and check pin DS2 again. If signal not present, the backplane is faulty.
	Wrong Grant Card	Make sure that G7272s, not G727s, are used on the bus.

Table 7-1 (cont'd)
Basic Troubleshooting Chart

SYMPTOM	CAUSE(S)	CORRECTIVE ACTION
"Dead" VSV11/VS11 (Cont'd)	Bad M7064 (if B-CLK present)	Replace M7064.
	Bad DW11 (VS11): Faulty M8217, M9403 or BC05L Cables	Verify that M7061 is receiving +12V (pin CD2). If not, verify that M9403 is receiving +15V (pin AS1); if not, adjust or replace mounting box power supply. If +15V is OK, adjust regulator on M9403. If adjustment does not fix problem, replace M9403. If problem persists, M9403 is faulty, so replace it. If problem persists, replace M8217, BC05L cables and M9403, in that order.
"Hung" VSV11/VS11 (all registers zero)	No Timing, bad M7061, bad M7064 or bad backplane	See actions for related items in previous table block (for "Dead" unit).
Tests 1-3 Fail: DPC Nonzero or DSR not 100000.	Bad M7064 Display Processor.	Replace M7064 module.
Tests 1-3 Fail: CSR Error Code = "DBUS Signal Hung" or "DBUS Data Read/Write Error"	Bad M7064	Disconnect DBUS cable from M7064; if problem persists, replace M7064 module.
	Bad DBUS Cable	Disconnect DBUS cable from all modules except M7064; if problem persists, swap DBUS Cable.
	Bad M7061: Channel Select jumpers wrong; or illegally driving DBUS.	Verify setup of W5 through W8; W5 and W6 must not both be IN, and W7 & W8 must not both be IN. If jumpers OK, disconnect DBUS cable from M7061; if this fixes problem, swap M7061.
	Bad M7062: Channel Select jumpers wrong; or illegally driving DBUS.	Verify setup of W3 through W6; W3 and W5 must not both be IN, and W4 and W6 must not both be IN. If jumpers OK, disconnect DBUS cable from M7062; if this fixes problem, swap M7062.

Table 7-1 (cont'd)
Basic Troubleshooting Chart

SYMPTOM	CAUSE(S)	CORRECTIVE ACTION
Tests 1-3 Fail: CSR Error Code = "VBUS Signal Hung"	Bad Module or Backplane	The VBUS is the C-D Interconnect on the backplane. Only the M7061 Sync Generator drives VBUS signals monitored by the M7064 Display Processor. However, any of the modules or the backplane could be shorting a signal or causing an open. The M7064 cannot run with any modules removed, so one module at a time must be swapped and the system retested. If the problem persists, check the backplane pins and slots for shorts and bad connections.
Tests 1-3 Fail: Any Error Code other than above, or incorrect register.	Bad M7064 Display Processor module	Replace M7064 module.
	Bad Timing from M7061	If External Sync is being used, adjust pot R48 on M7061. If problem persists, replace M7061 module.
Unexpected Joystick Switch Interrupt	Bad M7061 module	Replace M7061 module.
Errors in Tests 1-12	Bad M7064 module.	Replace M7064 module.
	Bad M8217 (VS11)	Replace M8217
Tests 13-15: Interrupt to wrong vector	Incorrect setup of vector switches on M7064 (E43).	Verify/Correct switches on E43.
	Bad M7064	Replace M7064

Table 7-1 (cont'd)
Basic Troubleshooting Chart

SYMPTOM	CAUSE(S)	CORRECTIVE ACTION
When running in DPU-Only Mode, any error in Tests 1-22	Bad M7064	Replace M7064
	Bad Timing from M7061 Sync Generator	If External Sync is being used, verify that signal is applied from VT100 or VRV02. If problem persists, adjust R48. If problem persists, replace M7061.
Tests 17-27: Image Memory SYNC Timeout (Not DPU-Only Mode)	Bad M7062 Image Memory	Verify that jumper W2 is IN on all M7062's; if it is, note the failing channel and swap M7062 modules in that channel one at a time.
	Bad DBUS Cable	Replace DBUS cable
Error in Test 23	Bad M7061	Note channel ir error and replace M7061 for that channel. If error is unexpected Switch interrupt or Flag, the H3060 Joystick or cable could be faulty.
	Bad DBUS Cable	Replace DBUS cable.
Tests 28-30: SYNC or DATA AVAILABLE Timeout or Hung DBUS Signal	Jumpers W1 and/or W2 not installed on M7062	Verify that W1 and W2 are installed on all M7062's.
	Bad M7062	Replace M7062
	Bad DBUS Cable	Replace DBUS Cable
	Bad M7064	Replace M7064
Test 28 or 30 Fails: Consistent Data Errors (Same RAM Group)	Bad M7062	Note the channel and data bits in error. Replace M7062; the bad module is determined by the Channel Select jumpers, W3 through W6, and the switches on E59; refer to Table 2-14 or 2-15.

Table 7-1 (cont'd)
Basic Troubleshooting Chart

SYMPTOM	CAUSE(S)	CORRECTIVE ACTION
Tests 28, 30: Random Data Errors	Bad Timing from M7061	If External Sync being used, verify that signal is applied from VT100 or VRV02. If problem persists, adjust R48. If problem persists, replace M7061.
Error in Test 29	Bad M7062 (Interlace Mode Control Logic)	Note the failing memory channel and replace M7062. If two M7062's are used in one channel, swap one at a time.
Test 32: No Display Present	Monitor faulty, video cable connections incorrect, or switches on E49 of M7062 not set	If the monitor is VRV02, refer to Table 7-2. If monitor is VT100, proceed as follows: Verify all video cable connections. Verify that the VT100 video circuitry is working by pressing SET-UP on the keyboard. If no display is present, adjust the Brightness control in the VT100; if display is still absent, consult the VT100 Technical Manual. If the SETUP frame appears, check the video cable by swapping one wire with another. Run Test 33 in the diagnostic. If only the cursor appears, the problem is in the M7062 Image Memory; verify the switches on E49 of all M7062's. If the switches are OK, swap the M7062. If the problem persists swap the M7061. If even the cursor does not appear, swap the M7061. If the problem persists, replace the VT100.
Tests 32-34: Display Rolls	Set-up of Monitor and M7061 not consistent	Verify that switch and jumper settings on M7061 for scan mode (Interlace/Non-Interlace) and frequency (60/50Hz) correspond to Keyboard SET-UP selections.
	Bad or Misadjusted M7061 Sync Generator	If Internal Sync mode is being used, swap the M7061. If External Sync mode is being

Table 7-1 (cont'd)
Basic Troubleshooting Chart

SYMPTOM	CAUSE(S)	CORRECTIVE ACTION
Tests 32-34: Display Rolls (Cont'd)		used (as with VT100 or VRV02), proceed as follows: Make sure external signal is being applied to M7061 from VT100 or VRV02 Keyboard Interface; check power & cables. With a display present, halt the CPU. Then adjust pot R48 on the M7061. If the display will not stabilize at any position of the pot, swap the M7061. If the problem persists, swap the video pigtail cable. If the problem still persists, the problem is in the monitor: refer to Table 7-2 if VRV02, or VT100 Technical Manual.
Test 32: Display Present and Stable but Data Missing	Bad M7062, M7061 or M7064	Replace M7062, M7061 or M7064, in that order.
Test 33: Cursor Appears but No Test Pattern Visible	Incorrect settings of switches on E49 of M7062	Verify switch settings. If problem persists, replace M7062.
Test 33: Cursor Drifts	Trimmers on H3060 Joystick not Adjusted	Using a small screwdriver, refer to Figure 2-26 and adjust Trimmers on the H3060. If the cursor drifts up or down, move the Vertical Balance Adj. (to the right of the joystick). If the cursor drifts to the left or right, move the Horizontal Balance Adj.
	Bad M7061 (Cursor Control, -5V Converter, Fuses)	Replace M7061

Table 7-1 (cont'd)
Basic Troubleshooting Chart

SYMPTOM	CAUSE(S)	CORRECTIVE ACTION
Test 33: No Switch or Match Interrupt When Switch Pressed	Bad Cable, H3060 Joystick, or M7061	Verify cable connections. If problem persists, replace H3060. If problem persists, replace M7061.
Test 35: Configuration Not As Expected	Incorrect Switch and Jumper Settings on M7062 and/or M7061	Verify Switch and Jumper settings.
	Bad M7061 or M7062	Replace M7061 or M7062.
Video too dim or too bright	Misadjusted Monitor	If monitor is VRV02, refer to Table 7-2. If monitor is VT100 adjust intensity via keyboard SET-UP with up and down arrow keys. If that adjustment is not sufficient, adjust the internal Brightness control.
	Pot R9 on M7061 Misadjusted	If the monitor is a VRV02, refer to Table 7-2. If the monitor is a VT100, adjust pot R9 counter-clockwise to increase the video amplitude or clockwise to decrease the amplitude. If necessary, readjust the brightness of the monitor, noting especially the relationship between keyboard video and graphics video. Several iterations may be required.
Test 33: Incorrect Cursor Size or Color	Incorrect Jumper Settings on M7061; or Bad M7061	Refer to Table 2-13 and verify that jumpers W10, W11, W16 and W17 are correctly set. If they are and the problem persists, swap the M7061.

Table 7-1 (cont'd)
Basic Troubleshooting Chart

SYMPTOM	CAUSE(S)	CORRECTIVE ACTION
Test 34: Incorrect Number of Shades/ Colors Present	Incorrect Settings of Switches on DIP Pack E49 on M7062.	Verify settings on E49; refer to Tables 2-14 or 2-15.
	Incorrect Connection of Video Cables	Verify connection of video cables.
	Incorrect Setting of W21 or W22 on M7061, or Bad M7061	Verify jumpers W21 and W22. If problem persists, replace M7061.
	Monitor Out of Adjustment	If the monitor is VRV02 refer to Table 7-2. If the monitor is VT100, adjust the brightness, as described in previous section.
Display Distorted or out of Focus	Monitor Out of Adjustment	If the monitor is VRV02, refer to Table 7-2. If the monitor is VT100, adjust the Vertical Linearity, Height, and Focus controls on the video board in the VT100 case.
Test 34: No Blink	Bad M7061	Replace M7061
Test 34: Incorrect Blink Rate	Incorrect Jumper Settings on M7061; or Bad M7061	Refer to Table 2-13 and verify that jumpers W12 through W14 are correctly set. If they are and the problem persists, swap the M7061.

Table 7-2
Video/VRV02 Monitor Troubleshooting Chart

SYMPTOM	CAUSE	CORRECTIVE ACTION
No raster.	No power.	Check power switch. Check power outlet. Check power cord.
No raster.	Color gun switches off in monitor.	Turn on the individual color gun control switches at the upper right corner of the monitor drawer.
No raster.	Monitor supply power limiting.	Disconnect video cables, turn contrast and brightness controls off. Cycle power switch once slowly and then slowly increase brightness. Reconnect video cables.
No raster.	Drawer connectors not connected.	Check all connectors in the drawer, at the power supply, and at the CRT tube neck.
No raster.	Broken or damaged wiring.	Check wires extending between drawer and the rest of the monitor for broken or chafed insulation. Especially examine the wiring for shorts or broken wires.
No raster.	Brightness controls misadjusted.	See adjustment for white balance.
No raster.	Blown fuse. Check fuse and replace. Find cause of blown fuse.	Check that the line voltage selection plug CN 802 is correct for the operating line voltage. A chart in the monitor manual details the proper power supply jumper selections. Check for wiring shorts or broken wires. Replace the monitor drawer. If it continues to blow fuses, replace the power supply. If it still blows fuses, replace the CRT.

Table 7-2 (cont'd)
Video and VRV02 Monitor Troubleshooting Chart

SYMPTOM	CAUSE	CORRECTIVE ACTION
No raster.	Failing drawer module or power supply.	Replace the drawer first, and then the power supply.
No video.	Contrast level too low.	Turn the Contrast control clockwise.
No video.	Monitor improperly cabled to M7061, or setup not consistent.	Connect the monitor cables as described in Chapter 2. Ensure that the M7061 switches are consistent for the requirements of the installation. For instance, if the VS/VSV11 is to be synchronized to an external source, the external source must be cabled, and the switches and jumpers of the M7061 module must be correctly set. If only one monitor is being driven by the VS/VSV11 the cables must be terminated with 75 ohms. If more than one monitor is being driven with the same cable, then the last monitor must be terminated and all others must be set to a high impedance input. Switch the impedance switch on the back of the VRV02 monitor to 75 OHMS or HIGH as necessary.
No video.	The color gun control switches in the monitor are off.	Turn the gun control switches in the monitor drawer on.
No video.	M7062 memory board switches off or improperly set.	Run the diagnostic Test 33, Manual Joystick Test. If the cursor is displayed, and is white (or the color selected by the jumpers on the M7061 module), but no memory data is displayed, then the video data is not getting to the M7061 module. The most likely cause for this would be the M7062

Table 7-2 (cont'd)
Video and VRV02 Monitor Troubleshooting Chart

SYMPTOM	CAUSE	CORRECTIVE ACTION
No video. CONT'D		switches closest to the edge fingers (E49). The switches at the top and bottom of the M7062 module should be set the same. See Chapter 2 for the proper switch selection. The switches at the top of the module are as important as those at the bottom, but the diagnostic can test the switches at the module top. The top switch settings can be verified by running Test 35 of the diagnostic. In the report, those video data bits which are active indicate closed switches.
No video from the keyboard.	The VIDEO OUT cable from the Keyboard Interface is missing or the cable has a broken wire, or the logic module in the Keyboard Interface is bad.	Connect the Keyboard Interface directly to the monitor, VIDEO OUT to Green input. Pressing SET-UP should present the familiar VT100 display in green on the CRT. If the display is not present, swap conductors within the video cable. If the display appears, replace the video cable. If still not present replace the keyboard interface module.
No video from the keyboard.	Pot R48 at the top edge of the M7061 module is set improperly.	Pressing SET-UP should present the familiar VT100 display in green on the CRT. If the VT100 display is present adjust pot R48 on the M7061 module (see Figure 2-7). Rotate it counter- clockwise to increase the keyboard video level. This pot also controls the gain of the external sync source amplifier. Too low a setting will cause random failures such as loss of sync. Increasing the setting further than necessary will cause failures in noisy environments because the M7061 will try to sync to the noise.

Table 7-2 (cont'd)
Video and VRV02 Monitor Troubleshooting Chart

SYMPTOM	CAUSE	CORRECTIVE ACTION
Keyboard video intensity is adequate, but graphics video is too dim.	Pot R9, half way down the M7061 module on the right side, may be set too low.	Rotate pot R9 counter-clockwise to increase the video amplitude. This must be done carefully, as this pot also affects the sync pulse amplitude. Rotating the pot counter- clockwise decreases the sync amplitude, and clockwise increases the sync amplitude. Decreasing the sync amplitude below a signal level of approximately 0.3 volts will cause the monitor to lose sync and the picture to roll. This pot can be set by performing the following procedure. Run Test 34 of the diagnostic, select display number 3, adjust the pot so that the right-most vertical stripe is white (See the section of this trouble-shooting chart dealing with white balance.) If the keyboard video is still too bright, decrease the keyboard video with pot R48 at the board edge.
No video.	The CRT color video gains are set too low.	The gains of the Red, Blue or Green video amplifiers of the monitor are adjustable. These controls can be found from the diagram on the monitor drawer cover/access panel. Do not adjust the BACKGROUND GAIN. Set these gains carefully. These controls set the color of the display. Increase the intensity of a specific color by rotating that amplifier's gain pot clockwise. If a gain pot is at the end of its travel and the display requires still more of this color, balance can be achieved by reducing the other two color gains.

Table 7-2 (cont'd)
Video and VRV02 Monitor Troubleshooting Chart

SYMPTOM	CAUSE	CORRECTIVE ACTION
No video or missing color.	Disconnected or bad video cable wire. Partially seated or bad switch on a M7062 memory module. Poorly seated memory or M7061 sync module. Poorly seated or bad DBUS cable.	Provided that the previous test in this table for the joystick cursor showed that the M7061 module was driving all three video cables, perform the following tests: Check the video cable wire connections for the color missing and reconnect. Test the wire continuity by swapping it with one of the other wires in the multiple conductor video cable. Re-seat the switches on the M7062 memory modules and verify their proper settings. The switches at both the top and bottom of each memory board should be set the same. Re-seat the memory and sync modules. The diagnostic can report a bad DBUS cable or connection. Seat the cable and re-test. If the problem persists swap the cable and re-test. Replace the cable or the memory module as necessary. The failing memory board in a Non-Interlaced system is the one addressed for that channel. The failing memory in an Interlaced system is one of two addressed for that channel. If the missing color is either red or blue replace the module with switches 5 and 6 closed. If the missing color is either of the green intensities replace the memory with switches 2 and 3 closed. It is unlikely that both or all bits of the display system would go bad at the same time so be sure to check memory module seating and switches. If after swapping modules and cables the data is still missing, it is possible that the backplane is bad.

Table 7-2 (cont'd)
Video and VRV02 Monitor Troubleshooting Chart

SYMPTOM	CAUSE	CORRECTIVE ACTION
No video or missing color. CONT'D		Vacuum the card slots and retry the modules. Examine the pins of the backplane connectors in the memory and the sync module slots. If warranted replace the backplane.
Video is missing from one or more particular pixels and the diagnostic may report an error in either memory set/clear or memory patterns test.	The memory may have a bad ram chip or the read circuitry is failing. The diagnostic will report errors from incorrect data read from the memory array. However, it is unable to detect errors in the data path from a point just before the bottom switches (E49) on the memory, through the backplane, through the sync module, to the display. If the diagnostic is not reporting errors but the display has missing data, the problem is most likely in this path.	Examine the error report listing of the diagnostic. Look for a specific address or ram bank which consistently errors. If you can identify a series of discrete addresses or one ram consistently in error replace the memory module. The module to be replaced is identified from the diagnostic error listing. Identify the memory channel. (A complete listing of the memory and sync channels can be obtained from the configuration type-out test of the diagnostic.) Use the charts in Chapter 2 to identify the memory channel jumper configuration for the memory channel which fails. If the system is configured Non-Interlaced, with 4 video data bits, only one M7062 module should assigned per channel. Check that there is only one and replace that module. If the system is configured Interlaced, the data bit(s) in error identify which memory of the two possible per channel is bad. If bits 9 or 8 error, replace the memory of the indicated channel which has it's switches 1,2,3, and 4 set. If bits 7 or 6 error replace the other module.

Table 7-2 (cont'd)
Video and VRV02 Monitor Troubleshooting Chart

SYMPTOM	CAUSE	CORRECTIVE ACTION
Video is missing from one or more particular pixels. CONT'D		If the diagnostic does not indicate an error and the screen has missing pixels, identify the missing color or shade. Use the monitor gun switches at the upper right corner of the monitor drawer to respectively turn only one or possibly two guns on at a time until the missing color or shade is identified. Check the cable and connections for that color. Identify the channel driving that monitor, and in sequence replace the memory and then the sync module. The memory module to be replaced is identified by its switch settings. If switches 3 and 4 are set that memory stores the most- and least- significant green bits, respectively. Switches 5 and 6 store red blue, respectively. (For monochrome displays switch 3 is the most significant bit and switch 6 is the least.) If swapping the memory does not restore the missing data swap the sync module. Finally, examine the backplane.
The display appears to be missing every other pixel on a horizontal line.	The daisy chained DBUS cable has a bad connection or a broken wire for the least significant data bus bit.	Reseat or replace the DBUS cable.
No sync: The image rolls vertically or horizontally.	The Sync Select switch at the monitor rear is set for External input.	Set the sync select switch to the Composite Sync (SYNC COMP.) input position. The monitor will now derive its sync signal from the Green input.

Table 7-2 (cont'd)
Video and VRV02 Monitor Troubleshooting Chart

SYMPTOM	CAUSE	CORRECTIVE ACTION
No sync: Picture rolls horizontally and vertically and shows no green.	The monitor may not be correctly wired either at the monitor or the M7061 module.	For a rapid check try the other two cables to see if one of them has green on it. Note that the VS/VSV must be generating a display to see "green". Run Test 34 of the diagnostic and select the Gun Identification display, selection 7.
No sync.	The system is configured for an external sync source and the source is not powered or not connected.	Power or connect the external sync source to the VS/VSV. This might be the Keyboard Interface.
No sync	The switches on the M7061 sync module are mis-set.	Check the switch settings and the jumper configuration and reseat the module. Any of the switches of the M7061 module can cause this problem except switch 10, which isn't used.)
No sync	The Keyboard user-selected functions differ from those selected by the M7061 sync board switches.	Select SETUP B on the Keyboard and specifically set the proper state for the Interlaced and 60 Hz functions. Refer to Chapter 2.
No sync	The external sync source is not RS-170 compatible.	The external sync source must have equalization pulses during its vertical sync pulse. It must also conform to the frequency variation tolerance of the RS-170 specification.
No sync	The M7061 sync output level is too low.	Adjust pot R9 on the right side and half way down the M7061 module clockwise to increase the sync amplitude. This, however, decreases the

Table 7-2 (cont'd)
Video and VRV02 Monitor Troubleshooting Chart

SYMPTOM	CAUSE	CORRECTIVE ACTION
No sync. CONT'D		video amplitude on the Composite Video (Monochrome/ Green) and VT100 Outputs. Adjust this pot with care. Too much either way and the image may roll.
No sync	The gain of the external sync source input amplifier on the M7061 is low.	Adjust pot R48 on the top edge of the M7061 sync module clockwise until either the raster of horizontal background lines on the monitor stabilizes or the pot has had 25 turns (to the end of its travel). Adjust the pot counter- clockwise until the raster stops rolling. Finally, adjust the pot clockwise until the display rolls, then back off the pot counter- clockwise by 3/4 turn. If the display occasionally rolls continue adjusting the pot gradually counter- clockwise. The display should roll and then stop each time the "80/132" (9) key is pressed while the keyboard is in SETUP mode. Should it not stop adjust the pot clockwise.
No sync: The display is sync'ed horizontally but rolls vertically.	The Vertical Hold pot of the monitor is misadjusted. The external sync source amplifier gain or the sync level out is at too low a level for the system to synchronize.	Disconnect the video cable on the Green monitor input. Adjust the Vertical Hold pot until the monitor raster is just barely rolling. Reconnect the Green cable. If the display still rolls but occasionally drops into sync readjust the monitor Vertical Hold. If the display rolls without change increase the output sync level by turning pot R9, at right side of the M7061 module, clockwise. This adjustment is nonlinear. The sync amplitude will increase then decrease as the pot is turned counter- clockwise from the end of its

Table 7-2 (cont'd)
Video and VRV02 Monitor Troubleshooting Chart

SYMPTOM	CAUSE	CORRECTIVE ACTION
No sync. CONT'D		clockwise limit. The video level will increase over the same pot travel. If the display continues to roll vertically but not horizontally, adjust the external sync source gain pot, R48, at the top edge of the M7061. This adjustment is covered in another section of this table.
The display rolls horizontally and vertically and no adjustment seems to change the rate.	No sync into the Green input of the monitor.	Connect the Keyboard Interface Video Output directly to the Green input of the VRV02. Adjust the Vertical and Horizontal Hold controls as necessary to get a stable display. If the display will not stabilize replace the Keyboard Interface source with a VT100 Vide Output source. If the monitc display is now stable replace the Keyboard Interface. If the display is not stable after again adjusting the Horizontal and Vertical Hold controls, replace the drawer of the VRV02. If the display can only be brought into sync when it is connected to the Keyboard Interface, either the video cabling or the M7061 sync module is bad. Use another conductor of the cable to verify the system connections. If the display still will not synchronize replace the M7061.
The display jitters.	The M7061 sync module switches and keyboard options are not set compatibly.	Set the Keyboard SETUP functions for the same configuration as the M7061 sync module switches. Refer to Chapter 2. Select SETUP B on the keyboard and set the proper state for the Interlace and 60 Hz functions. Check the state of the NONINTERLACE sig-

Table 7-2 (cont'd)
Video and VRV02 Monitor Troubleshooting Chart

SYMPTOM	CAUSE	CORRECTIVE ACTION
The display jitters. CONT'D		nal in the VSV/VS by running diagnostic Test 35 and observing the printout. If the sync module switches are correct, but the backplane signal does not reflect the switch setting, one of the other modules of the system or the backplane may be bad. Also try reseating the switches.
The display jitters.	The monitor Vertical Phase control is not adjusted properly for Interlaced operation.	Adjust the Vert Phase 2 control in the monitor drawer until the raster lines of the image are barely visible.
Display jitters; or large blank horizontal bars flash randomly on the display.	The monitor is probably being powered from an ac supply which has ground loop noise.	Power the monitor from the same supply as the host computer. If the bars are no longer present the previous ac power source was disrupting the display. Tie the computer power and the monitor power grounds together. If the bars are still present replace the M7061 sync module.
The display jitters.	The external sync source gain may be set too close to its upper or lower limit of control.	Adjust pot R48 on the top edge of the M7061 sync module clockwise. If the jitter gets worse adjust the pot counter-clockwise.
The display jitters.	The sync output level to the monitor may be low.	Adjust pot R9, halfway down the right side of the M7061 sync module, counter-clock-wise. Reverse direction if the jitter gets worse.
The display jitters.	The phase locked loop on the M7061 sync module cannot maintain lock.	Replace the M7061 module. If the new sync module also causes the display to jitter, replace the drawer of the VRV02.

Table 7-2 (cont'd)
Video and VRV02 Monitor Troubleshooting Chart

SYMPTOM	CAUSE	CORRECTIVE ACTION
Display is not centered.	The Vertical and Height controls of the monitor need adjustment.	Adjust the appropriate position controls in the VRV02 monitor drawer. The controls are labeled in the lower left corner of the monitor drawer.
Display is not centered.	The Vertical Blank, Horizontal Phase, and Horizontal Blank controls of the monitor need adjustment.	Adjust the appropriate controls in the VRV02 monitor drawer. The Vertical Blank control blanks or deletes greater or lesser amounts of the top of the screen. Set the Vertical Blank control so that when the monitor is displaying a Non-Interlaced image the first line of the display appears to start off screen. When the monitor is displaying an Interlaced image adjust the vertical blank so the first line starts in the top center of the screen. The Horizontal Phase control moves the display to the right or left. Adjusting the control to move the display to the right will eventually cause the image to wrap around on top of itself. The Horizontal Blank control will blank or delete greater or lesser amounts of the left edge of the screen.
Display size: The image is too big or too small.	The Vertical and Horizontal Size controls need adjustment.	Adjust the appropriate controls in the monitor. Adjust the Height control to make the image larger from top to bottom. Adjust the Width control to make the image wider from side to side.
Display size: The image is missing the top 20-30 lines.	Bad Vertical Blank circuit in monitor.	Replace the drawer of the VRV02 monitor.

Table 7-2 (cont'd)
Video and VRV02 Monitor Troubleshooting Chart

SYMPTOM	CAUSE	CORRECTIVE ACTION
Heat sensitivity of display size or jitter. Lines missing at top of display but not adjustable via Vertical Blank.	Heat sensitive Vertical Blank circuit: When the drawer is closed the problem will occur, and when the drawer is open and the circuit is cooler the missing lines might reappear.	Replace the monitor circuitry (VRV02 drawer).
Linearity: The image displayed bends inward or outward at the sides.	The Side Pincushion control may need adjustment.	Adjust the SP-C control in the VRV02 monitor drawer until the sides of the image appear vertical and straight.
Uneven display color or discolored lines.	External magnetic fields may have disrupted the purity of the color CRT. One of the three electron beams of the color tube in addition to hitting its own phosphor dots may be partially hitting one of the other phosphor colors as well.	To test for this condition, turn all three guns off, and then turn one gun on at a time. Look for patches shading the basic gun color. All three guns of the monitor must be driven from the same cable to eliminate possible cabling problems. Turn the brightness of the background up until it is visible. Sequentially, using the monitor drawer gun switches, turn only one gun on at a time. Look for shading of the base color. If shading is observed the monitor should be degaussed. Use the internal degaussing coil. Press the degaussing switch until all distortion leaves the screen, then release the switch.
Discolored lines.	Focus out of adjustment.	Adjust the Focus control in the monitor (at top right of power supply).

Table 7-2 (cont'd)
Video and VRV02 Monitor Troubleshooting Chart

SYMPTOM	CAUSE	CORRECTIVE ACTION
Uneven display color.	If the color is uneven because the image lacks green shading, the green Digital-to-Analog Converter (DAC) of the M7061 sync module may need adjustment. The levels may be saturating at the high or low ends of the DAC's range.	The M7061 sync module's Green output level is controlled by pot R9, half-way down the right side of the module. However, before adjusting that pot conduct the following test. Leave only the Green cable attached to the monitor. Run diagnostic Test 34 and select display 3. Fifteen vertical green bars should appear. They should be stepped in intensity, and the steps should be approximately even in intensity increase. If the steps appear as described go to the next trouble-shooting step. If the stepped increase is not even, adjust pot R9 on the M7061 module until the steps are even Care must be exercised when adjusting this pot, as it will also affect the level of the sync signal fed to the monitor. If the adjustment is too low and the sync signal is affected, the monitor image will tend to roll or lose sync. If this adjustment cannot be made replace the M7061.
Uneven display color.	The individual color gain controls of the monitor may need adjustment.	The red and blue cables carry binary (ON/OFF) data. The green cable carries four levels of voltage corresponding to off and three green intensities. The monitor has analog inputs and interprets the input voltage levels on the cables. It displays a color intensity proportional to the input voltage. The monitor response to the cable voltage is controlled by the individual color gain pots in the monitor drawer. These gain

Table 7-2 (cont'd)
Video and VRV02 Monitor Troubleshooting Chart

SYMPTOM	CAUSE	CORRECTIVE ACTION
Uneven display color. CONT'D		pots should be adjusted while a white image is displayed. Select Display 9 of Test 34 of the diagnostic. A square white image should appear on the screen. Adjust the monitor gain pots to restore the missing color, OR reduce the other two colors until the square is a close approximation to a gray-white. The monitor should now display images which are more closely color balanced. Tweak the pots for best balance with the images typically displayed. Also check the White Balance section of this trouble-shooting chart.
White balance: The image changes color as the brightness control is varied.	The background brightness controls of the monitor may need adjustment.	The following adjustment procedure should NOT be performed unless absolutely necessary. The necessity can be determined as follows. Select Display 9 of Test 34 of the diagnostic. Turn the Brightness and Contrast controls to their minimum settings. The monitor screen should be dark. If the screen is not dark perform the adjustment. Increase the Contrast control until the square image is at medium brightness. Increase the Brightness control setting until the background is just barely visible. Observe the square image as the brightness is increased. The image might change shade slightly. If the change is slight, most attempts at adjustment will only tend to increase the shade change. The controls will, however, allow the white balance to be restored. The adjustment procedure is a

Table 7-2 (cont'd)
Video and VRV02 Monitor Troubleshooting Chart

SYMPTOM	CAUSE	CORRECTIVE ACTION
White balance. CONT'D		series of iterations of the same adjustments. The adjustments tend to interact, and the serviceperson's color resolving ability will tire. Perform the following steps: Turn the Contrast and Brightness controls to their minimum settings. Turn the Brightness to its midpoint. Turn the following six controls in the monitor drawer to their minimum settings: RED BRIGHTNESS GAIN, BLUE BRIGHTNESS GAIN, GREEN BRIGHTNESS GAIN, RED BACKGROUND, BLUE BACKGROUND, and GREEN BACKGROUND. Slowly increase the RED BACKGROUND and GREEN BACKGROUND controls until the screen is just barely illuminated with yellow. It's best to perform this adjustment in a darkened area. If that is not possible shade the CRT face from stray reflections and excessive light. Shading the screen will allow closer determination of the color shades involved. Slowly increase the BLUE BACKGROUND control setting until the screen is just barely illuminated with gray. Increase the RED BRIGHTNESS GAIN and GREEN BRIGHTNESS GAIN controls until the screen is again just barely illuminated with yellow. When looking intensely at the screen for long periods, color determination tires. Look away occasionally. Now increase the BLUE BRIGHTNESS GAIN until the screen is again gray. Increase the external

Table 7-2 (cont'd)
Video and VRV02 Monitor Troubleshooting Chart

SYMPTOM	CAUSE	CORRECTIVE ACTION
White balance. CONT'D		brightness control and observe the display for color shading of the gray setting. If the color needs adjusting back to gray, turn the blue gun control switch off. Adjust the RED BRIGHTNESS GAIN and GREEN BRIGHTNESS GAIN until the screen is again yellow but at the new intensity setting. Turn the blue gun back on and readjust the screen to a gray shade. Reduce the external brightness control until the screen is at minimum illumination. Turn the blue gun control switch off. Adjust the RED BACKGROUND and GREEN BACKGROUND controls until the screen is again just barely illuminated with yellow. Turn the blue gun back on and adjust the BLUE BACKGROUND until the screen is again gray. Increase the external brightness and continue this procedure until the setting of the external brightness control has no effect on the screen color. Rapidly turning the external brightness down will cause the screen to briefly appear green as the long persistence phosphor decays. Ignore this effect. Always adjust from yellow to gray. The human eye is more sensitive to shades of yellow than shades of maroon or magenta. After the background white balance is satisfactory, see the section of the trouble-shooting chart concerning image color balance and contrast white balance.

7.5 M7061 SYNC ADJUSTMENT USING OSCILLOSCOPE

This paragraph descibes the initial adjustments to the M7061 Sync Generator module in VSV11/VS11-AP, -AR, -AS, and -AT systems to be made if an oscilloscope is available. For the best quality, it is highly recommended that an oscilloscope be obtained and the following proceedure performed.

Perform the following steps in order to adjust the M7061 Sync Generator module and VRV02-B monitor for initial operation, or when quality of the video signal is in doubt. Tektronix 465, 485 or equivalent oscilloscope should be available to aid in making the adjustments.

1. Make sure that power is ON to all components (computer system and monitor) and that the computer system is initialized.

2. Turn up the brightness and contrast controls on the front of the VRV02 display monitor and observe the screen. A raster (many fine parallel horizontal lines) should be observed. In addition, a "sync tab" (blanked block at the center of the lower edge of the screen) should be observed. Press SET-UP on the VRV02 keyboard; the standard set-up frame should be visible. If no raster or set-up frame is visible, recheck the cabling, monitor power, etc. (see Table 7-2)

3. Press SET-UP again. The screen should go blank. If video from the keyboard is still present, press SET-UP then the "0" (RESET) key to clear the screen.

4. Set up the oscilloscope as follows:

    a. Connect the Channel 1 probe to the second GREEN input of the VRV02 monitor (this input is in parallel with the input to which the signal cable for Green is connected).

    b. Select triggering from the Channel 1 source.

    c. Set the Channel 1 Vertical amplitude control at 0.10 volts per division X 1.

    d. Set the horizontal sweep at 20 microseconds per division.

    e. Set the trigger controls for AUTO triggering.

    f. Set vertical mode for Channel 1 only.

    g. Select AC coupling for channel 1.

    h. Select the negative slope for triggering.

i. Position the trace in the middle of the screen.

5. Initialize the processor and make sure that there is no picture on the monitor screen.

6. Adjust the trigger level until a stable display on the oscilloscope can be observed. The display should consist of several low-going pulses, each about 5 microseconds long. These are sync pulses.

7. Adjust potentiometer R48 on the M7061 module (Figure 2-7) to the center of its range (12.5 turns from either end).

8. Observe the amplitude of the low-going pulses on the oscilloscope. These should be 0.4 volts in amplitude.

9. If the amplitude of the low-going pulses is not 0.4 volts, adjust potentiometer R9 (clockwise to increase the sync level, and counter- clockwise to decrease it) on the M7061 module until the amplitude is correct. If the adjustment cannot be made using only R9, also adjust R48.

10. Press SET-UP on the VRV02 keyboard and observe the set-up frame on the monitor screen. The picture should be stable (no rolling, tearing, etc.). If the picture is not stable, and if the the sync amplitude has been adjusted according to the above procedure, the monitor requires adjustment; refer to Table 7-2.

11. Set the Brightness and Contrast controls on the front of the VRV02 monitor to the center of their range.

12. Load and start the VSV11/VS11 diagnostic program (CVVSA for PDP-11 and LSI-11 systems, EVTCB for VAX systems) and select Test 34 (Selected Displays). Refer to Chapter 2, Paragraph 2.5, for loading and running procedures.

13. Select display #5 (Crosshatch). Also make sure that the set-up frame is present on the screen.

14. Open the monitor drawer and, referring to the printed legend within the drawer, turn off the RED and BLUE guns, leaving only the GREEN gun on. The crosshatch pattern should be entirely green.

15. On the M7061 module, adjust potentiometer R48 until the intensity of the characters in the Set-Up frame and the intensity of the crosshatch are equal. Turning R48 counter-clockwise increases the video level of the set-up characters, while turning it clockwise decreases the video level of the set-up characters.

NOTE

Do not rotate R48 too far clockwise, as this will decrease the input gain too far and the M7061 may not be able to sync to the incoming signal.

16. If the two intensities cannot be made equal by adjusting only R48, adjust potentiometer R9. Turning R9 counter-clockwise increases the video level and decreases the sync level.

17. Initialze the processor to clear the crosshatch from the screen. Press the "0" key on the VRV02 keyboard to clear the set-up frame and all other VRV02-generated video from the screen.

18. Observe the oscilloscope display once again and, if necessary, adjust R9 to obtain a 0.4 volt amplitude on the sync pulses.

19. Repeat the previous steps, adjusting R48 and R9, until the crosshatch intensity matches the set-up frame intensity and the sync amplitude is 0.4 volt.

20. Turn the RED and BLUE guns back on via the switches in the monitor drawer to return the monitor to normal operating condition.

APPENDIX A

PARTS/DATA SHEETS

The following paragraphs list the mounting requirements, power requirements, and major hardware components for each VS11 and VSV11 model.

The paragraphs are arranged as follows:

Paragraph	Model No.
A. 1	VS11-AA, VS11-AB
A. 2	VS11-AC, VS11-AD
A. 3	VS11-AE, VS11-AF
A. 4	VS11-AH, VS11-AJ
A. 5	VS11-AP, VS11-AR
A. 6	VS11-AS, VS11-AT
A. 7	VSV11-AA, VSV11-AB
A. 8	VSV11-AC, VSV11-AD
A. 9	VSV11-AE, VSV11-AF
A. 10	VSV11-AH, VSV11-AJ
A. 11	VSV11-AP, VSV11-AR
A. 12	VSV11-AS, VSV11-AT

A.1 VS11-AA, -AB PARTS/DATA SHEET

Definition: UNIBUS Raster Graphics System with one Image Memory and without Display Monitor.

The VS11-AA (60 Hz) and VS11-AB (50 Hz) are identical; they differ only in switch settings on the M7061 Sync Generator Module to distinguish between 60 Hz and 50 Hz operation.

Parts List:

Qty.	Part No.	Description
1	M7061	Sync Generator/Cursor Control Module
1	M7062	Image Memory Module
1	M7064	Display Processor Module
1	H3060-A	Joystick Assembly (with Cable)
1	70-15987-0M	DBUS Data Cable (40-Conductor Flat Cable w/ 2 Taps)
1	70-15822-0	Joystick Pigtail Cable
1	17-00193-00	5-Conductor COAX Pigtail Cable
1	17-00192-00	25-Foot 4-Conductor COAX Monitor Cable
2	07272	Grant Continuity Card (LSI-11 Bus)
1	DW11-BK	UNIBUS to LSI-11 Bus Converter Assy.
(1)	(M8217)	(Bus Converter Module - Quad Height)
(1)	(M9403)	(Cable Connector Module)
(1)	(TEV11)	(LSI-11 Bus Terminator Module)
(1)	(BC05L-06)	(6-Foot 40-Conductor Flat Cable)
(1)	(DDV11-CK)	(4-Slot Hex-Height Backplane)
(1)	(70-16830)	(Power Harness Adapter Cable)

Mounting Requirements: Single (4-Slot) System Unit Mounting Space in BA11-K, -L, -F, or -P Mounting Box (for DDV11-CK); plus Quad-height SPC slot in UNIBUS backplane in same box as DDV11-CK.

Power Requirements: + 5 Vdc @ 9.0 Amp.
+15 Vdc @ 0.7 Amp.

A.2 VS11-AC, -AD PARTS/DATA SHEET

Definition: UNIBUS Raster Graphics System with two Image Memory modules and without Display Monitor.

The VS11-AC (60 Hz) and VS11-AD (50 Hz) are identical; they differ only in switch settings on the M7061 Sync Generator Module to distinguish between 60 Hz and 50 Hz operation.

Parts List:

Qty.	Part No.	Description
1	M7061	Sync Generator/Cursor Control Module
2	M7062	Image Memory Module
1	M7064	Display Processor Module
1	H3060-A	Joystick Assembly (with Cable)
1	70-15987-0M	DBUS Data Cable (40-Conductor Flat Cable w/ 2 Taps)
1	70-15822-0	Joystick Pigtail Cable
1	17-00193-00	5-Conductor COAX Pigtail Cable
1	17-00192-00	25-Foot 4-Conductor COAX Monitor Cable
2	07272	Grant Continuity Card (LSI-11 Bus)
1	DW11-BK	UNIBUS to LSI-11 Bus Converter Assy.
(1)	(M8217)	(Bus Converter Module - Quad Height)
(1)	(M9403)	(Cable Connector Module)
(1)	(TEV11)	(LSI-11 Bus Terminator Module)
(1)	(BC05L-06)	(6-Foot 40-Conductor Flat Cable)
(1)	(DDV11-CK)	(4-Slot Hex-Height Backplane)
(1)	(70-16830)	(Power Harness Adapter Cable)

Mounting Requirements: Single (4-Slot) System Unit Mounting Space in BA11-K, -L, -F, or -P Mounting Box (for DDV11-CK); plus Quad-height SPC slot in UNIBUS backplane in same box as DDV11-CK.

Power Requirements: + 5 Vdc @ 10.5 Amp.
+15 Vdc @ 1.2 Amp.

A.3 VS11-AE, -AF PARTS/DATA SHEET

Definition: UNIBUS Raster Graphics System with one Image Memory and 12" B/W Monitor w/ Keyboard.

The VS11-AE (120V/60Hz) and VS11-AF (240V/50Hz) differ in switch settings on the M7061 Sync Module (60/50 Hz), and in monitor power cord and setting of power selector switch.

Parts List:

Qty.	Part No.	Description
1	M7061	Sync Generator/Cursor Control Module
1	M7062	Image Memory Module
1	M7064	Display Processor Module
1	H3060-A	Joystick Assembly (with Cable)
1	70-15987-0M	DBUS Data Cable (40-Conductor Flat Cable w/ 2 Taps)
1	70-15822-0	Joystick Pigtail Cable
1	17-00193-00	5-Conductor COAX Pigtail C ble
1	17-00192-00	25-Foot 4-Cond. COAX Monitor Cable
2	07272	Grant Continuity Card (LSI-11 Bus)
1	DW11-BK	UNIBUS to LSI-11 Bus Converter Assy.
(1)	(M8217)	(Bus Converter Module - Quad Height)
(1)	(M9403)	(Cable Connector Module)
(1)	(TEV11)	(LSI-11 Bus Terminator Module)
(1)	(BC05L-06)	(6-Foot 40-Conductor Flat Cable)
(1)	(DDV11-CK)	(4-Slot Hex-Height Backplane)
(1)	(70-16830)	(Power Harness Adapter Cable)
1	VT100-LA (VS11-AE) or VT100-LB (VS11-AF)	Video Terminal, with 12" Black & White CRT, Detachable Keyboard, and Power Cord. (Make sure the Power Selector switch on the rear of the monitor case is properly set.)

Mounting Requirements: Single (4-Slot) System Unit Mounting Space in BA11-K, -L, -F, or -P Box; plus Quad-SPC slot in UNIBUS backplane in same box.

Power Requirements:

+5 Vdc @ 9.0 Amp.
+15 Vdc @ 0.7 Amp.
VT100-LA: 90-128 Vac @ 2.2 Amp., 1-Phase
VT100-LB: 180-256 Vac @ 1.1 Amp., 1-Phase

A.4 VS11-AH, -AJ PARTS/DATA SHEET

Definition: UNIBUS Raster Graphics System with two Image Memories and 12" B/W Monitor w/ Keyboard.

The VS11-AH (120V/60Hz) and VS11-AJ (240V/50Hz) differ in switch settings on the M7061 Sync Module (60/50 Hz), and in monitor power cord and setting of power selector switch.

Parts List:

Qty.	Part No.	Description
1	M7061	Sync Generator/Cursor Control Module
2	M7062	Image Memory Module
1	M7064	Display Processor Module
1	H3060-A	Joystick Assembly (with Cable)
1	70-15987-0M	DBUS Data Cable (40-Conductor Flat Cable w/ 2 Taps)
1	70-15822-0	Joystick Pigtail Cable
1	17-00193-00	5-Conductor COAX Pigtail Cable
1	17-00192-00	25-Foot 4-Cond. COAX Monitor Cable
2	G7272	Grant Continuity Card (LSI-11 Bus)
1	DW11-BK	UNIBUS to LSI-11 Bus Converter Assy.
(1)	(M8217)	(Bus Converter Module - Quad Height)
(1)	(M9403)	(Cable Connector Module)
(1)	(TEV11)	(LSI-11 Bus Terminator Module)
(1)	(BC05L-06)	(6-Foot 40-Conductor Flat Cable)
(1)	(DDV11-CK)	(4-Slot Hex-Height Backplane)
(1)	(70-16830)	(Power Harness Adapter Cable)
1	VT100-LA (VS11-AE) or VT100-LB (VS11-AF)	Video Terminal, with 12" Black & White CRT, Detachable Keyboard, and Power Cord. (Make sure the Power Selector switch on the rear of the monitor case is properly set.)

Mounting Requirements: Single (4-Slot) System Unit Mounting Space in BA11-K, -L, -F, or -P Box; plus Quad-SPC slot in UNIBUS backplane in same box.

Power Requirements:

+5 Vdc @ 10.5 Amp.
+15 Vdc @ 1.2 Amp.
VT100-LA: 90-128 Vac @ 2.2 Amp., 1-Phase
VT100-LB: 180-256 Vac @ 1.1 Amp., 1-Phase

A.5 VS11-AP, -AR PARTS/DATA SHEET

Definition: UNIBUS Raster Graphics System with onee Image Memory and 19" Color Monitor w/ Keyboard.

The VS11-AP (120V/60Hz) and VS11-AR (240V/50Hz) differ in switch settings on the M7061 Sync Generator Module (60/50 Hz) and in the power cords and power selectors on the monitor components (CRT & Keyboard Interface).

Mounting Requirements: Single (4-Slot) System Unit Mounting Space in BA11-K, -L, -F, or -P Box; plus Quad-SPC slot in UNIBUS backplane in same box.

Power Requirements:

+ 5 Vdc @ 9.0 Amp.
+15 Vdc @ 0.7 Amp.

VRV02-BA:	(CRT):	108-132 Vac @ 1.1 Amp. 1-Phase
(Keyboard Interface):		90-128 Vac @ 1.5 Amp., 1-Phase
VRV02-BB:	(CRT):	216-264 Vac @ 0.6 Amp. 1-Phase
(Keyboard Interface):		180-256 Vac @ 0.8 Amp., 1-Phase

[Parts List is on the following page]

Parts List:

Qty.	Part No.	Description
1	M7061	Sync Generator/Cursor Control Module
1	M7062	Image Memory Module
1	M7064	Display Processor Module
1	H3060-A	Joystick Assembly (with Cable)
1	70-15987-0M	DBUS Data Cable (40-Conductor Flat Cable w/ 2 Taps)
1	70-15822-0	Joystick Pigtail Cable
1	17-00193-00	5-Conductor COAX Pigtail Cable
1	17-00192-00	25-Foot 4-Cond. COAX Monitor Cable
2	G7272	Grant Continuity Card (LSI-11 Bus)
1	DW11-BK	UNIBUS to LSI-11 Bus Converter Assy.
(1)	(M8217)	(Bus Converter Module - Quad Height)
(1)	(M9403)	(Cable Connector Module)
(1)	(TEV11)	(LSI-11 Bus Terminator Module)
(1)	(BC05L-06)	(6-Foot 40-Conductor Flat Cable)
(1)	(DDV11-CK)	(4-Slot Hex-Height Backplane)
(1)	(70-16830)	(Power Harness Adapter Cable)
1	VRV02-BA (VSV11-AP) or VRV02-BB (VSV11-AR)	Color Video Terminal, with: 19" Color CRT, w/ Power Cord, Detachable Keyboard, Keyboard Interface w/ Power Cord, BC05F-15 15' Serial Interface Cable, Video Extension Cable, 20mA Loopback Test Connector

A.6 VS11-AS, -AT PARTS/DATA SHEET

Definition: UNIBUS Raster Graphics System with two Image Memories and 19" Color Monitor w/ Keyboard.

The VS11-AS (120V/60Hz) and VS11-AT (240V/50Hz) differ in switch settings on the M7061 Sync Generator Module (60/50 Hz) and in the power cords and power selectors on the monitor components (CRT & Keyboard Interface).

Mounting Requirements: Single (4-Slot) System Unit Mounting Space in BA11-K, -L, -F, or -P Box; plus Quad-SPC slot in UNIBUS backplane in same box.

Power Requirements:

+ 5 Vdc @ 10.5 Amp.
+15 Vdc @ 1.2 Amp.

VRV02-BA:	(CRT):	108-132 Vac @ 1.1 Amp. 1-Phase
	(Keyboard Interface):	90-128 Vac @ 1.5 Amp., 1-Phase
VRV02-BB:	(CRT):	216-264 Vac @ 0.6 Amp. 1-Phase
	(Keyboard Interface):	180-256 Vac @ 0.8 Amp., 1-Phase

[Parts List is on the following page]

Parts List:

Qty.	Part No.	Description
1	M7061	Sync Generator/Cursor Control Module
2	M7062	Image Memory Module
1	M7064	Display Processor Module
1	H3060-A	Joystick Assembly (with Cable)
1	70-15987-0M	DBUS Data Cable (40-Conductor Flat Cable w/ 2 Taps)
1	70-15822-0	Joystick Pigtail Cable
1	17-00193-00	5-Conductor COAX Pigtail Cable
1	17-00192-00	25-Foot 4-Cond. COAX Monitor Cable
2	G7272	Grant Continuity Card (LSI-11 Bus)
1	DW11-BK	UNIBUS to LSI-11 Bus Converter Assy.
(1)	(M8217)	(Bus Converter Module - Quad Height)
(1)	(M9403)	(Cable Connector Module)
(1)	(TEV11)	(LSI-11 Bus Terminator Module)
(1)	(BC05L-06)	(6-Foot 40-Conductor Flat Cable)
(1)	(DDV11-CK)	(4-Slot Hex-Height Backplane)
(1)	(70-16830)	(Power Harness Adapter Cable)
1	VRV02-BA (VSV11-AP) or VRV02-BB (VSV11-AR)	Color Video Terminal, with: 19" Color CRT, w/ Power Cord, Detachable Keyboard, Keyboard Interface w/ Power Cord, BC05F-15 15' Serial Interface Cable, Video Extension Cable, 20mA Loopback Test Connector

A.7 VSV11-AA, -AB PARTS/DATA SHEET

Definition: LSI-11 Bus Raster Graphics System with one Image Memory and without Display Monitor.

The VSV11-AA (60 Hz) and VSV11-AB (50 Hz) are identical; they differ only in switch settings on the M7061 Sync Generator Module to distinguish between 60 Hz and 50 Hz operation.

Parts List:

Qty.	Part No.	Description
1	M7061	Sync Generator/Cursor Control Module
1	M7062	Image Memory Module
1	M7064	Display Processor Module
1	H3060-A	Joystick Assembly (with Cable)
1	70-15987-0M	DBUS Data Cable (40-Conductor Flat Cable w/ 2 Taps)
1	70-15822-0	Joystick Pigtail Cable
1	17-00193-00	5-Conductor COAX Pigtail Cable
1	17-00192-00	25-Foot 4-Conductor COAX Monitor Cable
2	G7272	Grant Continuity Card (LSI-11 Bus)

Mounting Requirements: 3 Adjacent Quad-Height slots in H9273-A LSI-11 Bus Backplane (or Equivalent)

Power Requirements: + 5 Vdc @ 6.0 Amp.
+12 Vdc @ 0.7 Amp.

A.8 VSV11-AC, -AD PARTS/DATA SHEET

Definition: LSI-11 Bus Raster Graphics System with two Image Memory Modules and without Display Monitor.

The VSV11-AC (60 Hz) and VSV11-AD (50 Hz) are identical; they differ only in switch settings on the M7061 Sync Generator Module to distinguish between 60 Hz and 50 Hz operation.

Parts List:

Qty.	Part No.	Description
1	M7061	Sync Generator/Cursor Control Module
2	M7062	Image Memory Module
1	M7064	Display Processor Module
1	H3060-A	Joystick Assembly (with Cable)
1	70-15987-0M	DBUS Data Cable (40-Conductor Flat Cable w/ 2 Taps)
1	70-15822-0	Joystick Pigtail Cable
1	17-00193-00	5-Conductor COAX Pigtail Cable
1	17-00192-00	25-Foot 4-Conductor COAX Monitor Cable
2	07272	Grant Continuity Card (LSI-11 Bus)

Mounting Requirements: 4 Adjacent Quad-Height slots in H9273-A LSI-11 Bus Backplane (or Equivalent)

Power Requirements: + 5 Vdc @ 7.5 Amp.
+12 Vdc @ 1.2 Amp.

A.9 VSV11-AE, -AF PARTS/DATA SHEET

Definition: LSI-11 Bus Raster Graphics System with one Image Memory and with 12" Monochrome (B/W) Display Monitor w/ Detachable Keyboard.

The VSV11-AE (120V/60Hz) and VSV11-AF (240V/50Hz) are functionally identical; they differ in switch settings on the M7061 Sync Generator Module to distinguish between 60 Hz and 50 Hz operation, and in the power cord and power selector switch on the monitor.

Parts List:

Qty.	Part No.	Description
1	M7061	Sync Generator/Cursor Control Module
1	M7062	Image Memory Module
1	M7064	Display Processor Module
1	H3060-A	Joystick Assembly (with Cable)
1	70-15987-0M	DBUS Data Cable (40-Conductor Flat Cable w/ 2 Taps)
1	70-15822-0	Joystick Pigtail Cable
1	17-00193-00	5-Conductor COAX Pigtail Cable
1	17-00192-00	25-Foot 4-Cond. COAX Monitor Cable
2	Q7272	Grant Continuity Card (LSI-11 Bus)
1	VT100-LA (VSV11-AE) or VT100-LB (VSV11-AF)	Video Terminal, with 12" Black & White CRT, Detachable Keyboard, and Power Cord. (Make sure the Power Selector switch on the rear of the monitor case is properly set.)

Mounting Requirements: 3 Adjacent Quad-Height slots in H9273-A LSI-11 Bus Backplane (or Equivalent)

Power Requirements:

+ 5 Vdc @ 6.0 Amp.
+12 Vdc @ 0.7 Amp.
VT100-LA: 90-128 Vac @ 2.2 Amp., 1- Phase
VT100-LB: 180-256 Vac @ 1.1 Amp., 1-Phase

A.10 VSV11-AH, -AJ PARTS/DATA SHEET

Definition: LSI-11 Bus Raster Graphics System with two Image Memory modules and 12" Monochrome (B/W) Display Monitor w/ Detachable Keyboard.

The VSV11-AH (120V/60Hz) and VSV11-AJ (240V/50Hz) are functionally identical; they differ in switch settings on the M7061 Sync Generator Module to distinguish between 60 Hz and 50 Hz operation, and in the power cord and power selector switch setting on the monitor.

Parts List:

Qty.	Part No.	Description
1	M7061	Sync Generator/Cursor Control Module
2	M7062	Image Memory Module
1	M7064	Display Processor Module
1	H3060-A	Joystick Assembly (with Cable)
1	70-15987-0M	DBUS Data Cable (40-Conductor Flat Cable w/ 2 Taps)
1	70-15822-0	Joystick Pigtail Cable
1	17-00193-00	5-Conductor COAX Pigtail Cable
1	17-00192-00	25-Foot 4-Cond. COAX Monitor Cable
2	07272	Grant Continuity Card (LSI-11 Bus)
1	VT100-LA (VSV11-AH) or VT100-LB (VSV11-AJ)	Video Terminal, with 12" Black & White CRT, Detachable Keyboard, and Power Cord. (Make sure the Power Selector switch on the rear of the monitor case is properly set.)

Mounting Requirements: 4 Adjacent Quad-Height slots in H9273-A LSI-11 Bus Backplane (or Equivalent)

Power Requirements:

+5 Vdc @ 7.5 Amp.
+12 Vdc @ 1.2 Amp.
VT100-LA: 90-128 Vac @ 2.2 Amp., 1- Phase
VT100-LB: 180-256 Vac @ 1.1 Amp., 1-Phase

A.11 VSV11-AP, -AR PARTS/DATA SHEET

Definition: LSI-11 Bus Raster Graphics System with one Image Memory and with 19" Color Display Monitor w/ Keyboard.

The VSV11-AP (120V/60Hz) and VSV11-AR (240V/50Hz) differ in switch settings on the M7061 Sync Generator Module (60/50 Hz) and in the power cords and power selectors on the monitor components (CRT & Keyboard Interface).

Parts List:

Qty.	Part No.	Description
1	M7061	Sync Generator/Cursor Control Module
1	M7062	Image Memory Module
1	M7064	Display Processor Module
1	H3060-A	Joystick Assembly (with Cable)
1	70-15987-0M	DBUS Data Cable (40-Conductor Flat Cable w/ 2 Taps)
1	70-15822-0	Joystick Pigtail Cable
1	17-00193-00	5-Conductor COAX Pigtail Cable
1	17-00192-00	25-Foot 4-Cond. COAX Monitor Cable
2	G7272	Grant Continuity Card (LSI-11 Bus)
1	VRV02-BA (VSV11-AP) or VRV02-BB (VSV11-AR)	Color Video Terminal, with: 19" Color CRT, w/ Power Cord, Detachable Keyboard, Keyboard Interface w/ Power Cord, BC05F-15 15' Serial Interface Cable, Video Extension Cable, 20mA Loopback Test Connector

Mounting Requirements: 3 Adjacent Quad-Height slots in H9273-A LSI-11 Bus Backplane (or Equivalent)

Power Requirements:

+5 Vdc @ 6.0 Amp.
+12 Vdc @ 0.7 Amp.

VRV02-BA: (CRT): 108-132 Vac @ 1.1 Amp. 1-Phase
(Keyboard Interface): 90-128 Vac @ 1.5 Amp., 1-Phase

VRV02-BB: (CRT): 216-264 Vac @ 0.6 Amp. 1-Phase
(Keyboard Interface): 180-256 Vac @ 0.8 Amp., 1-Phase

A.12 VSV11-AS, -AT PARTS/DATA SHEET

Definition: LSI-11 Bus Raster Graphics System with two Image Memories and 19" Color Display Monitor w/ Keyboard.

The VSV11-AS (120V/60Hz) and VSV11-AT (240V/50Hz) differ in switch settings on the M7061 Sync Generator Module (60/50 Hz) and in the power cords and power selectors on the monitor components (CRT & Keyboard Interface).

Parts List:

Qty.	Part No.	Description
1	M7061	Sync Generator/Cursor Control Module
1	M7062	Image Memory Module
1	M7064	Display Processor Module
1	H3060-A	Joystick Assembly (with Cable)
1	70-15987-0M	DBUS Data Cable (40-Conductor Flat Cable w/ 2 Taps)
1	70-15822-0	Joystick Pigtail Cable
1	17-00193-00	5-Conductor COAX Pigtail Cable
1	17-00192-00	25-Foot 4-Cond. COAX Monitor Cable
2	07272	Grant Continuity Card (LSI-11 Bus)
1	VRV02-BA (VSV11-AP) or VRV02-BB (VSV11-AR)	Color Video Terminal, with: 19" Color CRT, w/ Power Cord, Detachable Keyboard, Keyboard Interface w/ Power Cord, BC05F-15 15' Serial Interface Cable, Video Extension Cable, 20mA Loopback Test Connector

Mounting Requirements: 4 Adjacent Quad-Height slots in H9273-A LSI-11 Bus Backplane (or Equivalent)

Power Requirements:

+5 Vdc @ 7.5 Amp.
+12 Vdc @ 1.2 Amp.

VRV02-BA: (CRT): 108-132 Vac @ 1.1 Amp. 1-Phase
(Keyboard Interface): 90-128 Vac @ 1.5 Amp., 1-Phase

VRV02-BB: (CRT): 216-264 Vac @ 0.6 Amp. 1-Phase
(Keyboard Interface): 180-256 Vac @ 0.8 Amp., 1-Phase

APPENDIX B

VRV02-BA/BB 20MA TO EIA CONVERSION

The Keyboard Interface unit used in the VRV02-BA/BB consists of standard VT100 logic plus the VT1XX-AA 20mA Option. The VRV02-BA/BB is therefore supplied set up for 20mA Current Loop serial communications, and the EIA ("COMM.") connector is not active. If the unit is to interface to an EIA RS-232 communications line, the 20mA option must be disabled, as follows:

1. Open the case of the Keyboard Interface unit.

2. Disconnect the 20mA option board by removing the 8-inch 5-conductor interconnect cable. This cable runs from a connector on the narrow VT1XX-AA 20mA option board to a connector on the main VT100 logic module.

3. Tape the cable just removed securely to the bottom of the case for use in the event of a future requirement.

4. Reassemble the Keyboard Interface case and attach the EIA communications line to the "COMM." connector on the unit.

APPENDIX C

VT100/VRV02 SETUP AND OPERATOR INFORMATION

This Appendix is a brief overview of the procedures used to "set-up" the internal parameters of the VT100 or VRV02 for operation as a VSV11/VS11 graphics terminal. For detailed operating procedures, consult the VT100 User Guide, EK-VT100-UG.

The operating parameters of interest when using the VT100 or VRV02 as a graphics terminal are:

1. Interlace/Non-Interlace Scanning Mode,
2. 50Hz/60Hz Operating Frequency, and
3. Video Intensity.

Also of importance are the parameters necessary for serial communication with the host computer (Transmit/Receive Speed, Parity, etc.). There are other parameters which can be set-up as desired for operator convenience or host software compatibility.

The parameters are set using the SET-UP function of the keyboard. The following steps should be used to set up the Graphics-related operating parameters:

1. Press the SET-UP key in the upper left corner of the keyboard; the SET-UP A display should be seen on the screen. This display allows tab stops to be set; it does not affect graphic operation.
2. Observe the labels next to the top row of keys (the number keys) and press SETUP A/B (the "5" key); the SET-UP B display should appear on the screen.
3. The SET-UP B display allows the operating parameters to be set-up. In this display, four groups of four binary digits each should be seen, along with a T (Transmit) SPEED and R (Receive) SPEED indication. The blinking cursor should also be seen, initially at the left of the screen.

4. To set-up the Interlace/Non-Interlace mode of operation, use the space bar to move the cursor to the right until it is under the last (4th) digit of the third group. The state of this digit controls the Interlace/Non-Interlace scanning mode. If it is 0, the mode is Non-Interlaced. If it is 1, the mode is Interlaced. Determine which mode is to be used (it must match the set-up on the M7061 Sync Generator). The state of the digit, and hence the mode, is changed by pressing the TOGGLE 1/0 key (the "6" key).

5. To set-up the 50Hz/60Hz operating frequency, use the space bar to move the cursor to the right until it is under the last (4th) digit of the fourth group. The state of this digit controls the operating frequency. If the digit is 0, the terminal is set for 60Hz operation; if it is 1, it is set for 50Hz operation. Determine which frequency is to be used (it must match the set-up of the M7061 Sync Generator). The state of the digit, and hence the frequency, is changed by pressing the TOGGLE 1/0 key (the "6" key).

6. The Transmit and Receive Speeds (serial baud rates) can be changed by operating the TRANSMIT SPEED ("7" key) and RECEIVE SPEED ("8" key) keys.

7. The video intensity of the VT100-LA/LB can be adjusted up or down by pressing the Up-Arrow or Down-Arrow keys, respectively, at the upper right of the main keyboard. [The video cannot be adjusted in this manner on the VRV02 color monitor].

8. When set-up is complete, press the "8" key simultaneously with the SHIFT key to store the current parameters.

9. Exit the SET-UP mode by pressing the SET-UP key.